INSTITUTE OF AERONAUTICAL ENGINEERING
Dundigal, Hyderabad - 500 043

ELECTRICAL AND ELECTRONICS ENGINEERING

QUESTION BANK

Course Name	:	SWITCHING THEORY AND LOGIC DESISN
Course Code	:	A40407
Class	:	II B. Tech
Branch	:	EEE
Year	:	2016 – 2017
Course Coordinator	:	Mr S.Rambabu
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OBJECTIVES

To meet the challenge of ensuring excellence in engineering education, the issue of quality needs to be addressed, debated and taken forward in a systematic manner. Accreditation is the principal means of quality assurance in higher education. The major emphasis of accreditation process is to measure the outcomes of the program that is being accredited.

In line with this, Faculty of Institute of Aeronautical Engineering, Hyderabad has taken a lead in incorporating philosophy of outcome based education in the process of problem solving and career development. So, all students of the institute should understand the depth and approach of course to be taught through this question bank, which will enhance learner's learning process.

1. Group - A   (Short Answer Questions)

S. No	QUESTION	Blooms Taxonomy Level	Course Outcome
	UNIT-I **NUMBER SYSTEMS AND BOOLEAN ALGEBRA AND SWITCHING FUNCTIONS**		
1	Write short notes on binary number systems.	Remember	1
2	Discuss 1's and 2's complement methods of subtraction.	Understand	1
3	Discuss octal number system.	Understand	1
4	State and prove transposition theorem.	Remember	2
5	Show how do you convert AND logic to NAND logic?	Apply	3
6	Describe a short note on five bit bcd codes.	Remember	1
7	Illustrate about unit –distance code? State where they are used.	Apply	1
8	State about error correcting codes?	Remember	1
9	When do you say that a signal is asserted?	Understand	1
10	State about logic design and what do you mean by positive logic	Remember	2

S. No	QUESTION	Blooms Taxonomy Level	Course Outcome
	system?		

UNIT-II
MINIMIZATION AND DESIGN OF COMBINATIONAL CIRCUITS

S. No	QUESTION	Blooms Taxonomy Level	Course Outcome
1	Define K-map?	Remember	5
2	Write the block diagram of 2-4 and 3-8 decoders?	Understand	6
3	Define magnitude comparator?	Remember	6
4	What do you mean by look-ahead carry?	Remember	6
5	Simplify the Boolean function $x'yz + x'yz' + xy'z' + xy'z$ using K-map	Remember	5
6	How combinatorial circuits differ from sequential circuits?	Remember	6
7	What are the IC components used to design combinatorial circuits with MSI and LSI?	Understand	6
8	Define the importance of prime implications	Remember	5
9	Locate the minters in a three variable map for $f=\sum m(0,1,5,7)$	Remember	5
10	Simplify the Boolean function $x'yz + x'yz' + xy'z' + xy'z$ without using K-map	Apply	5

UNIT-III
SEQUENTIAL MACHINES FUNDAMENTALS

S. No	QUESTION	Blooms Taxonomy Level	Course Outcome
1.	What do you mean a stable state?	Remember	7
2.	What is a Flip-Flop?	Understand	7
3.	What are the applications of Flip-Flops?	Remember	7
4.	Express your view about synchronous latch?	Understand	7
5.	How do you build a latch using universal gates?	Apply	7
6.	What is the flip-flop memory characteristic?	Understand	7
7.	Distinguish between synchronous and asynchronous latch?	Remember	7
8	What is meant by clocked flip-flop?	Remember	7
9.	Why a gated D latch is called a transparent latch?	Remember	7
10.	What are the two types of flip-flops?	Remember	7
11	Explain about Different types of Latches in detail	Remember	7
12	Explain about S-R (NOR gates) Latch?	Remember	7
13	Explain about S-R (NAND gates) Latch?	Remember	7
14	Draw The truth table of gated D-Latch?	Apply	7
15	Distinguish between Latch and Flip Flop?	Remember	7
16	Draw The block diagram of sequential circuit?	Apply	7
17	Determine the output state of S-R latch (active low) for S=1, R=0, Q_n =1	Apply	7
18	What is Asynchronous sequential Circuit?	Remember	7
19	Draw the gated S-R latch Logic Diagram?	Apply	7
20	Determine the output state of S-R latch (active low) for S=0, R=0, Q_n =1	Understand	7
21	What is binary cell?	Remember	7
22	Draw The gated D-Latch logic diagram?	Apply	7

S. No	QUESTION	Blooms Taxonomy Level	Course Outcome
23	Determine the output state of gated D-latch for D=1, $Q_{n=0}$, enable=0.		7
24	Draw the S-R Latch(NAND) Truth Table ?	Apply	7
25	Determine the output state of JK flip-flop for J=1, K=1, $Q_{n=1}$ when clock is inactive.	Understand	7
26	Determine the output state of JK flip-flop for J=0, K=1, $Q_{n=1}$ when clock is active.	Understand	7
27	Determine the output state of S-R latch (active low) for S=0, R=1, $Q_n=1$	Understand	7
28	Draw the S-R latch (NOR) Truth Table ?	Apply	7
UNIT-IV SEQUENTIAL CIRCUIT DESIGN AND ANALYSIS			
1.	What are Shift registers?	Remember	8
2.	Distinguish between a shift register and counter?	Understand	8
3.	What are the applications of shift registers?	Remember	8
4.	Discuss about a bidirectional shift register?	Understand	8
5.	Summarize about a dynamic shift register?	Understand	8
6.	Describe about UART?	Understand	8
7.	Classify of counters?	Understand	8
8.	What are the advantages and disadvantages of ripple counters?	Remember	8
9.	What do you mean by terminal count?	Remember	8
10.	State variable modulus counter?	Remember	8
UNIT-V SEQUENTIAL CIRCUITS & ALGORTHMIC STATE MACHINES			
1.	What are the capabilities and limitations of FSM?	Understand	9
2.	Demonstrate about successor?	Understand	9
3.	Describe about terminal state?	Understand	9
4.	Define a strongly connected machine?	Remember	9
5.	List the advantage of having equivalent states?	Remember	9
6.	State 'state equivalence theorem'.	Understand	9
7.	Tell about distinguishing sequence?	Remember	9
8.	Define state compatibility?	Understand	9
9.	Describe a merger graph?	Understand	9
10.	State FSM compatibles?	Remember	9

2. Group - II   (Long Answer Questions)

S. No	Question	Blooms Taxonomy Level	Course Outcome
	UNIT-I **NUMBER SYSTEMS AND BOOLEAN ALGEBRA AND SWITCHING FUNCTIONS**		
1.	(a) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend: i. 100 – 110000 ii. 11010 - 1101. (b) Construct a table for 4 -3 -2 -1 weighted code and write 9154 using this code Write short notes on binary number systems.	Understand	1
2.	(a) Perform arithmetic operation indicated below. Follow signed bit notation: i. 001110 + 110010 ii. 101011 - 100110. (b) Explain the importance of gray code	Understand	1
3.	Find $(3250 - 72532)_{10}$ using 10's complement	Understand	1
4.	As part of an aircraft's functional monitoring system, a circuit is required to indicate the status of the landing gears prior to landing. Green LED display turns on if all three gears are properly extended when the \gear down" switch has been activated in preparation for landing. Red LED display turns on if any of the gears fail to extend properly prior to landing. When a landing gear is extended, its sensor produces a LOW voltage. When a landing gear is retracted, its sensor produces a HIGH voltage. Implement a circuit to meet this requirement	Apply	1
5.	(a) Divide 01100100 by 00011001 (b) Given that $(292)10 = (1204)b$ determine `b'	Understand	1
6.	(a) What is the gray code equivalent of the Hex Number 3A7 (b) Find the biquinary of number code for the decimal numbers from 0 to 9 (c) Find 9's complement $(25.639)_{10}$	Understand	1
7.	(a) Find (72532 - 03250) using 9's complement. (b) Show the weights of three different 4 bit self complementing codes whose only negative weight is - 4 and write down number system from 0 to 9.	Understand	1
8.	Decimal system became popular because we have 10 fingers. A rich person On earth has decided to distribute Rs.one lakh equally to the following persons from various planets. Find out the amount each one of them will get in their respective currencies: A from planet VENUS possessing 8 fingers B from planet MARS possessing 6 fingers C from planet JUPITER possessing 14 fingers D from planet MOON possessing 16 fingers	Apply	1

S. No	Question	Blooms Taxonomy Level	Course Outcome
9.	State and prove any 4 Boolean theorems with examples	Remember	2
10.	(a) Simplify to a sum of 3 terms: A'C'D' +AC' +BCD + A'CD' + A'BC + AB'C' (b) Given AB' + AB = C, Show that AC' + A'C = B	Apply	3
UNIT-II **MINIMIZATION AND DESIGN OF COMBINATIONAL CIRCUITS**			
1.	A combinational circuit has 4 inputs(A,B,C,D) and three outputs(X,Y,Z)XYZ represents a binary number whose value equals the number of 1's at the input i Find the minterm expansion for the X,Y,Z ii. Find the maxterm expansion for the Y and Z	Apply	5
2.	A combinational circuit has four inputs (A,B,C,D), which represent a binary-coded-decimal digit. The circuit has two groups of four outputs - S,T,U,V (MSB digit) and W,X,Y,Z.(LSB digit)Each group represents a BCD digit. The output digits represent a decimal number which is five times the input number. Write down the minimum expression for all the outputs.	Apply	5 & 6
3.	Simplify the following Boolean expressions using K-map and implement them using NOR gates: (a) F (A, B, C, D) = AB'C' + AC + A'CD' (b) F (W, X, Y, Z) = W'X'Y'Z' + WXY'Z' + W'X'YZ + WXYZ.	Understand	5
4.	Design BCD to Gray code converter and realize using logic gates	Understand	6
5.	Design 2*4 decoder using NAND gates	Understand	6
6.	Reduce the following expression using Karnaugh map (B 'A + A'B + AB')	Understand	5
7.	Design a circuit with three inputs(A,B,C) and two outputs(X,Y) where the outputs are the binary count of the number of "ON" (HIGH) inputs	Apply	6
8.	A certain 4 input gate called LEMON gate realizes the switching function LEMON (A,B,C,D) = BC(A+D). Assuming that the input variables are available in both primed and unprimed form: show a realization of the function $f(w,x,y,z)=\sum(0,1,6,9,10,11,14,15)$ with only three LEMON gates and one OR gate. Can all switching functions be realized with LEMON/OR logic	Apply	6
9.	Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7.	Apply	6
10.	Implement Half adder using 4 NAND gates.	Apply	6
UNIT-III **SEQUENTIAL MACHINES FUNDAMENTALS**			
1.	Analyze the clocked sequential circuits.	Understand	7

S. No	Question	Blooms Taxonomy Level	Course Outcome
2.	Examine with the help of a block diagram, the basic components of a Sequential Circuit?	Remember	7
3.	Compare RS and JK flip-flops.	Understand	7
4.	Describe about T – Flip-flop with the help of a logic diagram and characteristic table. Derive a T-flip-flop from JK and D flip-flops.	Understand	7
5.	Define Latch. Explain about Different types Of Latches?	Remember	7
6.	Explain about all flip flops in detail with diagram	Remember	7
7.	Derive the characteristic equations for all Flip-Flops.	Remember	7
8.	Memorize about basic macro cell logic diagram and explain.	Remember	7
9.	Differentiate combinational and sequential circuits	Understand	7
10.	Explain the working principle of JK Flip-Flop in detail.	Understand	7

UNIT-IV
SEQUENTIAL CIRCUIT DESIGN AND ANALYSIS

S. No	Question	Blooms Taxonomy Level	Course Outcome
1.	Explain the design of Sequential circuit with an example. Show the state reduction, state assignment	Remember	8
2.	Explain Serial Transfer in 4-bit shift Registers	Remember	8
3.	Explain about Binary Ripple Counter	Understand	8
4.	Define BCD Counter and Draw its State table for BCD Counter	Remember	8
5.	Explain the state reduction and state assignment in designing sequential circuit. Consider one example in the above process	Understand	8
6.	Design a sequential circuit with two D flip-ops A and B. and one input x. when x=0, the state of the circuit remains the same. When x=1,the circuit goes through the state transition from 00 to 11 to 11 to 10 back to 00.and repeats	Apply	8
7.	Design a Modulo-12 up Synchronous counter Using T-Flip Flops and draw the Circuit diagram	Apply	8
8.	Explain the Ripple counter design. Also a decade counter design	Remember	8
9.	Write short notes on shift register? Mention its application	Remember	8
10.	Design a left shift and right shift for the following data 10110101	Apply	8

UNIT-V
SEQUENTIAL CIRCUITS & ALGORTHMIC STATE MACHINES

S. No	Question	Blooms Taxonomy Level	Course Outcome
1.	Differentiate between Race free and Latch free design?	Understand	9
2.	Draw the ASM chart to count the number of ones in a register?	Apply	9
3.	Draw the ASM chart for a binary multiplier?	Apply	9
4.	Explain the concept of ASM chart?	Understand	9
5.	Obtain the primitive flow table for the circuit with two inputs, x1 and x2, and two outputs, z1 and z2,that satisfy the following four conditions: a. When x1x2 = 00, the output is z1z2 = 00. b. When x1 = 1 and x2 changes from 0 to 1, the output is z1z2 = 01.	Apply	9

S. No	Question	Blooms Taxonomy Level	Course Outcome
	c. When x2 = 1 and x1 changes from 0 to 1, the output is z1z2 = 10. d. Otherwise the output does not change.		

6.	An asynchronous sequential circuit is described by the excitation function
	$Y = x1x'2 + (x1 + x'2)y$ and the output function $z = y$.
	    a. Draw the logic diagram of the circuit.
	    b. Derive the transition table and output map.
	    c. Obtain a two state flow table.
		Apply	9

7.	Find the circuit that has no static hazards and implements the Boolean function $F(A, B, C, D) = \Sigma(0, 2, 6, 7, 8, 10, 12)$.	Apply	9
8.	Draw the ASM chart for adding or subtracting the two signed magnitude numbers A and B?	Remember	9
9.	Write the differences between Mealy and Moore type machines.	Understand	9
10.	A sequential circuit has 2 inputs w1=w2 and an output z. It's function is to compare the i/p sequence on the two i/p's. If w1=w2 during any four consecutive clock cycles, the circuit produces z=1 otherwise z=0 w1= 0110111000110 w2= 1110101000111 z=0000100001110	Apply	9

3. Group - III   (Analytical Questions)

S.No	QUESTIONS	Blooms Taxonomy Level	Course Outcome
	UNIT-I **NUMBER SYSTEMS AND BOOLEAN ALGEBRA AND SWITCHING FUNCTIONS**		
1.	Convert $(4085)9$ into base-5?	Apply	1
2.	Write the first 20 decimal digits in base 3?	Understand	1
3.	Write the steps involved in unsigned binary subtraction using complements with examples	Remember	1
4.	How do you perform addition of two signed binary number? Explain with examples.	Remember	1
5.	Differentiate between binary code and BCD code?	Understand	1
6.	How binary values are stored in memory? Explain	Understand	1
7.	Write the Axiomatic Definitions of Boolean Algebra.	Remember	2
8.	Write a table stating all the postulates and theorems of Boolean Algebra that are required for Logic minimization	Remember	2
9.	Convert $f(x)= x + y'z$ into canonical form	Understand	3
10	Differentiate between positive and negative logic.	Understand	4
	UNIT-II		

S.No	QUESTIONS	Blooms Taxonomy Level	Course Outcome
MINIMIZATION AND DESIGN OF COMBINATIONAL CIRCUITS			
1.	Implement the Boolean function F = AB + CD + E using NAND gates only.	Understand	5 & 6
2.	Simplify the Boolean function F(w, x, y, z) = Σ(1, 3, 7, 11, 15) + d(w, x, y, z) = Σ(0. 2, 5)	Apply	5
3.	Realize the logic diagram of a full subtractor using only 2-input NAND gates	Apply	6
4.	Realize the logic diagram of a full subtractor using only 2-input NOR gates	Apply	6
5.	Use a multiplexer having three data select inputs to implement the logic for the function F = Σ (0, 1, 2, 3, 4, 10, 11, 14, 15)	Apply	6
6.	Identify all the prime implicants and essential prime implicants of the following functions Using karnaugh map. F(A,B,C,D) = Σ(0,1,2,5,6,7,8,9,10,13,14,15).	Apply	5
7.	Construct a 4 to 16 line decoder using 2 to 4 line decoders	Apply	6
8.	Design a 4-bit Combinational circuit which generates the output as 2's complement of input binary number. Show that the circuit can be constructed with EX-OR gates	Apply	6
9.	Design a combinatorial circuit that converts a decimal digit from 2,4,2,1 code to the 8,4,-2,-1 code?	Understand	6
10	Design a combinatorial circuit that accepts a three bit number and generates an output Binary number equal to the square of the input number?	Understand	6
UNIT-III **SEQUENTIAL MACHINES FUNDAMENTALS**			
1.	Explain the operation of SR Flip-Flop using asynchronous inputs with truth table.	Remember	7
2.	Explain the Flip-Flop operating characteristics in detail	Remember	7
3.	Draw the schematic circuit of an edge triggered flip-flop with "active low preset" and "active low clear" using NAND gats and explain its operation	Understand	7
4.	Convert a JK FF to i) SR ii) T iii) D	Understand	7
5.	Convert a SR FF to i) JK ii) D iii) T	Understand	7
6.	Convert a D FF to i) JK ii)SR iii) T	Understand	7
7.	Convert a T FF to i) JK ii) D iii) SR	Understand	7
8.	Discuss the applications of flip-flops	Remember	7
9.	Give the transition table for the following flip-flops i) SR FF ii) D FF	Understand	7
10	Give the transition table for the following flip-flops i) JK FF ii) T FF	Understand	7
UNIT-IV **SEQUENTIAL CIRCUIT DESIGN AND ANALYSIS**			
1.	How many decade counters are required to convert a clock of 10	Understand	8

S.No	QUESTIONS	Blooms Taxonomy Level	Course Outcome
	MHz to 100 Hz?		
2.	What do you mean by presetting the counter?	Remember	8
3.	Assume that a 4-bit ripple counter is holding the count 0100.What will be the count after 29 pulses?	Understand	8
4.	What do you mean by resetting the counter?	Understand	8
5.	Compare state diagram and state table?	Remember	8
6.	What do you mean by initial state and final state?	Understand	8
7.	How do you test for the problem of lockout of a counter? How do you eliminate this problem?	Apply	8
8.	Generate the pulse train 100110 using indirect logic	Apply	8
9.	Design a type-D counter that goes through the states 0,2,4,6,0,…The undesired states must always go to a 0 on the next clock pulse?	Apply	8
10	Design a 3bit up/down counter which counts up when control signal M=1 and counts down when M=0.	Apply	8
UNIT-V SEQUENTIAL CIRCUITS & ALGORTHMIC STATE MACHINES			
1.	Explain the operations in microwave oven and construct the ASM chart for them.	Apply	9
2.	Design a synchronous state machine to generate following sequence of states. Represent the machine by a state diagram /ASM chart and display the onset of state 7(111) with the help of LED(use jk flip-flops).	Apply	9
3.	Draw an ASM chart for a 2 bit binary counter having one enable line E such that E=1(counting enabled) E=0(Counting disabled).	Apply	9
4.	Show that 8 exit paths in an ASM block emanating from the decision boxes that check the eight possible binary value of three control variables x,y,z.	Apply	9
5.	Draw the ASM chart of binary multiplier and design the control circuit using each of the following methods a)JK FF and gates. b)D FF and decoder	Apply	9
6.	Design control logic circuit using multiplexers.	Understand	9
7.	Draw the ASM chart for a 3 bit up-down counter.	Understand	9
8.	Draw the ASM chart for SR Flip-Flop.	Understand	9
9.	Draw the ASM chart for JK Flip-Flop.	Understand	9
10	Design a mod 5 counter using multiplexers.	Understand	9

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