INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

Department of Electrical and Electronics Engineering

QUESTION BANK

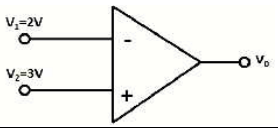
Course Name	**:**	**IC APPLICATIONS**
Course Code	**:**	**A50423**
Class	**:**	**III B. Tech I Semester**
Branch	**:**	**Electrical and Electronics Engineering**
Year	**:**	**2017 – 2018**
Course Faculty	**:**	**Mr. R Gangadhar Reddy, Assistant Professor, ECE**

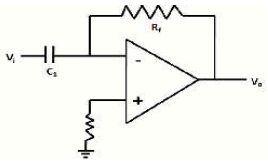
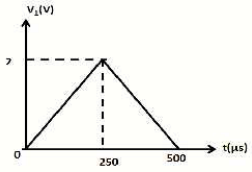
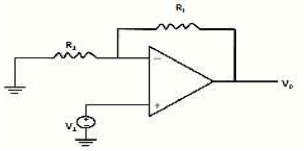
OBJECTIVES:

To meet the challenge of ensuring excellence in engineering education, the issue of quality needs to be addressed, debated and taken forward in a systematic manner. Accreditation is the principal means of quality assurance in higher education. The major emphasis of accreditation process is to measure the outcomes of the program that is being accredited.

S. No	QUESTION	Blooms Taxonomy Level	Program Outcome
	UNIT - I **INTEGRATED CIRCUITS**		
	Part – A (Short Answer Questions)		
1	Sketch and explain the basic CMOS inverter circuit	Understanding	1
2	Discuss about MOS transistor as Switch?	Analyze	1
3	Explain why NMOS transistor produces weak ‘1’ and PMOS transistor produces weak ‘0’?	Analyze	1
4	Discuss the characteristics of CMOS family	Analyze	1
5	Sketch and explain the circuit of two input CMOS NAND gate	Remember	1
6	Memorize why shift registers are considered basic memory devices? What is the	Understand	1
7	Describe non – inverting gates	Remember	1
8	Sketch two input NAND gate	Understand	1
9	Sketch and explain the circuit of two input CMOS NOR gate	Remember	1
10	Explain the concept of Fan-in and Fan-out	Understand	1
11	Discuss CMOS logic levels	Remember	1
12	Explain the concept of sinking and sourcing current	Remember	1
13	Define schottky transistor? Why it is used in logic families	Understand	1
14	Define i) DC noise margin ii) fanout	Remember	1
15	Discuss short note on diode logic	Understand	1
16	Sketch and explain 2- input TTL NOR gate	Evaluate	1
17	Explain the operation of AND gate using diode logic	Evaluate	1
18	Explain the operation of OR gate using diode logic	Remember	1
	Part – B (Long Answer Questions)		
1	Construct and explain the two input TTL NOR gate	Apply	1
2	Sketch and explain the CMOS OR-AND- INVERT gate	Apply	2
3	Explain with neat diagram interfacing of a TTL gate driving CMOS gates and vice Versa	Understand	2

4	Sate the rules for interfacing 5V TTL logic families	Knowledge	1
5	Differentiate TTL, CMOS, and ECL families	Analyze	2
6	Sketch and explain the circuit diagram of 2 – input CMOS NOR/OR gate	Apply	1
7	Discuss the characteristics of CMOS family	Understand	1
8	Explain about the salient features of schotttky TTL family. Give typical values of various parameters compare this logic family with that of standard TTL family	Understand	1
9	Constructs a transistor circuit of 2 inputs CMOS NAND gate. Explain the operation with the help of functional table	Apply	1
10	Differentiate CMOS , TTL and ECL with reference to logic levels, noise margin, propagation delay, fan out	Analyze	2
11	Explain function of a 3 state TTL gate	Understand	1
12	Explain the following terms i)Logic levels ii) D.C noise margin iii) fan out	Understand	1
13	Compare TTL and MOS logic families	Understand	1
14	Give the TTL families and compare them with reference to propagation delay, power consumption, speed power product and low level input current	Understand	1
15	Construct a 3 input NAND gate using diode logic and a transistor inverter. Analyze circuit with the help of transfer characteristics	Apply	1
16	Explain sinking current and source current of TTL output	Understand	1
17	Sketch the circuit diagram of basic TTL NAND gate and explain the 3 parts with the help of functional operation	Apply	1
Part – C (Analytical Questions)			
1	Use a combination of CMOS gates to generate the following functions. a) Z = A (buffer) b) Z = A. /B+/A.B (XOR)	Understand	2
2	Construct a CMOS transistor circuit that has the functional behaviour f(z)= $\overline{A.(B+C)}$	Apply	2
3	Sketch the resistive of a CMOS inverter and explain its behaviour for low and high outputs	Apply	2
4	Construct a CMOS transistor circuit that has the functional behaviour f(z)= ~~(A+B).(B+C)~~	Apply	2
5	Explain hoe to estimate sinking current for low output and sourcing current for high output of CMOS gate	Understand	1
6	Explain about CMOS open drain output	Understand	1
7	Explain the effect of floating inputs on CMOS gate	Understand	1
8	Construct a CMOS transistor circuit that has functional behaviour f(z)= ~~(A+$\overline{B}$)(B+C)~~	Apply	2
9	Sketch the logic diagram equivalent to the internal structure of an 2 input CMOS NAND gate	Apply	2
10	Expalin what is the use of decoupling capacitors	Understand	1
11	Construct a 3 input NAND gate using diode logic and a transistor inverter. Analyze circuit with the help of transfer characteristics	Apply	2
12	Explain sinking current and source current of TTL output	Apply	2
13	Sketch the circuit diagram of basic TTL NAND gate and explain the 3 parts with the help of functional operation	Apply	2
14	Discuss logic levels and noise margin for 74LS logic family	Apply	2
15	Explain why IC industry is moving toward low power supply voltage	Apply	2
UNIT - II OP-AMP AND APPLICATIONS			
Part – A (Short Answer Questions)			

1	Define op - amp	Understanding	2
2	What is the value of Vo in the circuit given in the figure below? 	Analyze	2
3	Explain if the open loop gain of an op-amp is very large, does the closed loop gain depend upon the external components of the op-amp?	Analyze	2
4	Why is RE replaced by a constant current bias circuit in a differential amplifier?	Analyze	2
5	Define common-mode-rejection ratio ?	Evaluate	2
6	Define slew rate. What causes the slew rate?	Analyze	2
7	Discuss why do we use Rcomp resistor?	Remember	2
8	The transient response rise time of an op-amp is 0.07μs. Find the small signal band width	Remember	2
9	What is the value of CMRR for an emitter coupled differential amplifier when RE is infinite	Understand	2
10	Classify the characteristics of ideal op- amp	Analyze	2
11	Explain active load is used	Understand	2
12	Discuss about practical op amp with neat sketch	Understand	2
13	Explain the difference between constant current bias and current mirror	Understand	2
14	Explain what is the input impedance of a non inverting op amp amplifier	Understand	2
15	Discuss the limitations of linear voltage regulators	Analyze	2
	Part – B (Long Answer Questions)		
1	List the characteristics of an ideal op-amp	Create	2
2	Explain low frequency small signal analysis of differential amplifier using hybrid p model.	Evaluate	2
3	Sketch a sample and hold circuit. Explain its operation and indicate its value	Evaluate	2
4	Differentiate between saw tooth wave and triangular wave	Analyze	2
5	List the non ideal characteristics of an op amp	Analyze	2
6	List the parameters that are important for AC applications	Evaluate	2
7	List the non-ideal DC characteristics of an O-amp. Explain any two.	Understand	2
8	Define offset voltage and offset current as referred to an OPAMP. How are these controlled in a practical non inverting amplifier. Explain with circuit diagrams and analysis	Evaluate	2
9	Discuss the following i) input offset voltage ii) CMRR	Understand	2
10	Discuss the frequency response of an op amp	Evaluate	2
11	Define SLEW RATE. How does this limit the response of an OPAMP? How can the slew rate be improved	Evaluate	2
12	What is Thermal drift? How does it affect the performance of an OPAMP	Understand	2
13	Explain with neat circuit diagram, how the following parameters of the OPAMP can be measured. i) CMRR ii) Slew Rate iii) offset Voltage	Understand	2
14	Sketch and explain the operation of triangular wave generator	Understand	2
15	Define an instrumentation amplifier? sketch a system whose gain is controlled by	Understand	2
	Part – C (Analytical Questions)		
1	Apply the input offset voltage of an OPAMP is 10mV dc. For a non Inverting amplifier with Rf= 10k and R= 1 k. What is the maximum Possible output offset voltage?	Evaluate	2
2	Find R1 and Rf in the lossy integrator so that the peak gain is 20 dB and the gain is 3dB down from its peak when = 10000 rad/sec, use a capacitance of 0.01μF	Evaluate	2

3	A Schmitt trigger with the upper threshold level VUT= 0V and hysteresis width VH=0.2V converts a 1KHz sine wave of amplitude 4Vpp into a square wave	Evaluate	2
4	Design an inverting amplifier with a gain of -5 and an input resistance of 10kΩ	Evaluate	2
5	Design a non inverting amplifier with a gain of 10	Evaluate	2
6	Design a square wave of peak amplitude of 500 mV has to be amplified to peak to peak amplitude of 3 volts with a rise time of 4μs or less. Can a 741 be used	Create	2
7	How fast can the output of an op amp by 10v, if its slew rate is 1V/ μs	Apply	2
8	Find the maximum frequency for a sine wave output voltage of 10v peak with an op amp whose slew rate is1V/ μs	Evaluate	2
9	Design an op amp differentiator that will differentiate an input signal with f max=100 Hz	Evaluate	2
10	Sketch the output wave form for a sine wave of 1V peak at 100Hz applied to the differentiator	Evaluate	2
11	The input VL to a differentiator of figure A. is shown in figure B. Find the output Vo if Rf = 2K and C1 = 0.1μF  	Evaluate	2
12	Solve the non-inverting amplifier of fig 11, R1=1K and Rf=10K. Calculate the maximum output offset voltage due to Vios and IB. The op-amp is LM307 with Vios=10mV and IB=300nA, Ios=50nA. Also calculate the value of Rcomp needed to reduce the effect of Op-amp IB. 	Evaluate	2
13	Discuss the function of voltage regulators	Analyze	2
14	Sketch the functional block diagram of 723 regulator	Remember	2
15	Explain the characteristics of three terminal IC regulators	Remember	2
	UNIT - III **ACTIVE FILTERS AND OSCILLATORS**		
	Part – A (Short Answer Questions)		
1	Define an electric filter	Analyze	3
2	Classify filters	Remember	3
3	Discuss advantages of passive filters	Remember	3
4	Explain why active filters are preferred	Analyze	3
5	Give the list commonly used filters	Analyze	3
6	Define pass band stop band of filter	Remember	3
7	Discuss why do we use higher order filters	Analyze	3
8	State the two conditions of oscillators.	Analyze	3
9	Differentiate between a saw-tooth wave and a triangular wave?	Evaluate	3
10	Define Butterworth, chebyshev filters	Analyze	3
11	Discuss the advantages of active filters over passive ones	Analyze	3
12	Describe the important parameters of a band pass filters	Analyze	3
13	Define switched capacitor? Discuss its impotance	Analyze	3
14	Define VCO? Give two applications that requires a VCO	Evaluate	3
15	Classify oscillators	Evaluate	3
	Part – B (Long Answer Questions)		
1	Sketch the circuit of a second order active high pass filter explain its working.	Create	3

2	Construct and derive the expression for first order low pass butter worth filter	Evaluate	3
3	Explain the operation of TWIN – T notch filter with a neat diagram.	Evaluate	3
4	Explain the operation of Narrow band pass filter with a neat diagram.	Analyze	3
5	Sketch the circuit diagram of second order low pass butter worth filter	Evaluate	3
6	Sketch and explain first order high pass butter worth filter	Evaluate	3
7	Explain the operation of wide band pass filters	Evaluate	3
8	Sketch the circuit diagram of narrow band pass filter and explain its operation	Remember	3
9	Classify the band reject filters	Understand	3
10	Construct the circuit diagram of wide band reject filter	Understand	3
11	Explain the working operation of narrow band reject filter	Understand	3
12	Construct the circuit of all pass filters	Analyze	3
13	Define phase shift oscillator and explain its operation with neat diagram	Remember	3
14	Explain the working operation of Wien bridge oscillator sketch with neat diagram	Evaluate	3
15	Sketch the output voltage capacitive voltage of the square wave generators	Understand	3
Part – C (Analytical Questions)			
1	Design a first order low pass filter for a high cut off frequency of 2KHz and pass band gain of 2	Create	3
2	Determine the order of the butter worth low pass filter so that at ω=1.5ω3-db, the magnitude response is done by at least 30db	Evaluate	3
3	Design a wide band reject filter having fh=400hz and fl= 2KHz having pass band gain as 2	Evaluate	3
4	Sketch and explain functional block diagram of NE 566	Analyze	3
5	Design a band pass filter so that f0 = 2KHz, Q = 20 and A0 = 10. Choose C=1µF.	Analyze	3
6	Design a phase shift oscillator for f=1KHz. The op-amp is a 741 with supply voltage ±15V.	Evaluate	3
7	Design a Wien bridge oscillator for f=1KHz. The op-amp is a 741 with supply voltage ±15V	Evaluate	3
8	Design a 50 Hz active notch filter	Evaluate	3
9	Design a second order butter worth high pass filter having lower cut off frequency 1KHz	Evaluate	3
10	Design a wien bridge oscillator uses R=4.7kΩ,C=0.01µf,and RF=2R1,what is the frequency of oscillation	Evaluate	3
11	Sketch the output voltage capacitive voltage of the square wave generators	Analyze	3
12	Construct the circuit and wave forms of triangle wave generator	Analyze	3
13	Differentiate swatooth and triangle wave generator	Analyze	
UNIT - 1V TIMER AND PHASE LOCKED LOOPS			
Part – A (Short Answer Questions)			
1	List the basic building blocks of a PLL. Draw the block schematic of PLL.	Analyze	4
2	What is a VCO? Give two applications that require a VCO.	Understand	4
3	Explain the role of low pass filter and VCO in PLLs.	Understand	4
4	What is the Butterworth response?	Analyze	4
5	Classify two basic modes in which the 555 timer operates?	Apply	4
6	What must be the relationship between the pulse width tp and the period T	Remember	4
7	Define duty cycle D	Understand	4
8	Discuss phase locked loop	Analyze	4
9	List the basic building blocks of the discrete PLL	Apply	4
10	Differentiate between the small signal and power amplifiers	Remember	4
11	List important features of the 555 timer	Understand	4
12	Give one application each in which the 555 can be used as a monostable and astable	Analyze	4
13	Give the applications of the PLL	Apply	4
14	Discuss what are available packages in 555 timer	Remember	4

15	Classify the modes of operation of a timer	Understand	4
Part – B (Long Answer Questions)			
1	Discuss and derive the expression for time delay of a monostable multivibrator	Understand	4
2	Discuss some applications of timer in monostable mode	Understand	4
3	Construct the circuit of Schmitt trigger using 555 timers and explain its operation.	Apply	4
4	Sketch and explain IC565	Apply	4
5	Sketch the circuit of an op-amp monostable multivibrator and explain its operation.	Apply	4
6	Explain the following for a phase locked loop.	Understand	4
7	Explain in detail any two application of PLL	Understand	4
8	Calculate output frequency f0, lock range fL and capture range fc of a 565 PLL if RT = 10KO, CT=0.01µF and C = 10 µF	Analyze	4
9	Construct the circuit of a Schmitt trigger using 555 timer and explain its operation	Apply	4
10	Explain a digital phase detector with necessary waveforms.	Understand	4
11	Derive the expression for Lock-in Range of IC 565 PLL.	Understand	4
12	Sketch the circuit of a PLL AM detector and explain its operation	Apply	4
13	Sketch the circuit of second order low pass filter and derive its transfer function	Apply	4
14	Explain the operation of IC 555 Timer in Astable mode with necessary diagrams	Understand	4
15	Explain the operation of IC 555 Timer in Monostable mode with necessary diagrams	Understand	4
Part – C (Analytical Questions)			
1	Design a monostable multivibrator using 555 timer to produce a pulse width of 100 ms verify the values of R and C obtained from the graph	Create	4
2	Calculate output frequency f0,lock range Δfc of a 565 PLL if Rt=10kΩ, Ct= 0.01 µf	Analyze	4
3	Construct free running ram generator circuit and output wave forms	Understand	4
4	An AstableMultivibrator has RA = 2.2KO, RB = 6.8KO and C = 0.01µF. Calculate (i) t HIGH (ii) t LOW (iii) free running frequency (iv) duty cycle D	Apply	4
5	An op-amp multivibrator circuit is constructed using the following components. R1 = 35kΩ,R2 = 30kΩ, R = 50kΩ and C = 0.01uF. Calculate the	Apply	4
6	An Astable 555 Oscillator is constructed using the following components, R1 = 1kΩ, R2 = 2kΩ and capacitor C = 10uF. Calculate the output frequency from the 555 oscillator and the duty cycle of the output waveform.	Apply	4
7	Calculate an Astable Multivibrators circuit is required to produce a series of pulses at a frequency of 500Hz with a mark-to-space ratio of 1:5. If R2 = R3 = 100kΩ's, calculate the values of the capacitors, C1 and C2required.	Analyze	4
8	Evaluate the 7805C voltage regulator, design a current source that will deliver a 0.25-A current to a 48 Ω,10W load	Evaluate	4
9	Design a adjustable voltage regulator to satisfy the following specifications output voltage Vo=5 to 12v ,output current Io=1.0A voltage regulator is LM317	Create	4
10	Explain the operation of Analog Phase detector using Balanced modulator.	Create	4
11	Discuss the drawbacks of Analog phase detector using Electronic switch.	Analyze	4
12	Discuss the operation of a FSK generator using 555 timer	Understand	4
13	Explain how is an astable multivibrator connected into a pulse position	Apply	4
14	Discuss the applications of PLL	Apply	4
15	Discuss what are available packages in 555 timer	Apply	4
UNIT - V D TO A AND A TO D CONVERTERS			
Part – A (Short Answer Questions)			
1	Explain the basic D/A techniques	Understand	5
2	Sketch the circuit diagram of multiplying DACs explain its operation	Analyze	5

3	Define monolithic DAC and design 1408 D/A converter	Understand	5
4	What is the principle of switch-mode power supplies? Discuss its advantages.	Understand	5
5	Discuss servo tracking A/D converter with its wave form	Understand	5
6	Why is an inverted R-2R ladder network DAC better than R-2R ladder DAC?	Understand	5
7	Which is the fastest ADC and why?	Analyze	5
8	Name the essential parts of a DAC.	Understand	5
9	List the various A?D conversion techniques	Remember	5
10	Calculate the values of the LSB and MSB for an 8bit DAC for the 0 to 10V range	Remember	5
11	Classify DACs on the basis of their output	Understand	5
12	Discuss name the essential parts of a DAC	Understand	5
13	Describe the various types of electronic switches used in D/A converter	Understand	5
14	Explain how many resistors are required in a12 bit weighted resistor DAC	Understand	5
15	Discuss why is an inverted R-2R ladder network DAC better than R-2R ladder	Understand	5
Part – B (Long Answer Questions)			
1	Explain the important specification of D/A and A/D converters	Understand	5
2	Explain the counter type A/D converter with the output waveform	Understand	5
3	Find the voltage at all nodes 0, 1, 2,…. And at the output of a 5-bit R-2R ladder DAC. The least Significant bit is 1 and all other bits are equal to 0. Assume VR = -10V and R=10K	Analyze	5
4	A dual slope ADC uses an 18 bit counter with a 5MHz clock. The maximum integrator input voltage in +12V and maximum integrator output voltage at 2n count is -10V. If R=100KO, find the size of the capacitor to be used for integrator.	Apply	5
5	Explain inverted R-2R ladder DAC.	Understand	5
6	Design an adjustable regulator from the 7810 regulator to get an output voltage of 15V.	Create	5
7	Design a current limit circuit for a 723 regulator to limit the current to 60mA	Create	5
8	Calculate the values of R1 and R2 for a high voltage 723 regulator, so as to get an output voltage of 28V.	Analyze	5
9	Classify the limitations of three terminal regulators? How to overcome these limitations? Explain the necessary circuits.	Analyze	5
10	Explain current fold back characteristics. Explain the current limit protection circuit.	Understand	5
11	What is the function of voltage regulator and mention the different types of voltage regulators	Understand	5
12	Name the different blocks of a series OPAMP voltage regulator and explain.	Understand	5
13	Discuss the role of the OPAMP in a voltage regulator	Analyze	5
14	Give the standard circuit representation of a three terminal monolithic regulator.	Apply	5
15	Mention and explain the characteristics of three terminal IC regulators.	Understand	5
Part – C (Analytical Questions)			
1	Calculate basic step of 9 bit DAC is 10.3 mV. If 000000000 represents 0V, what output produced if the input is 101101111	Evaluate	5
2.	Calculate the values of the LSB,MSB and full scale output for an 8 bit DAC for the 0 to 10V range	Evaluate	5
3	An ADC converter has a binary input of 0010 and an analog output of 20mv. What is the resolution	Evaluate	5
4	A given 4-bit digital to analog converter has a reference voltage of 15 volts and a binary in out of 0101. What is the proportionality factor	Evaluate	5
5	What output voltage would be produced by a D/A converter whose output range is 0 to 10 V and whose input binary number is i) 10 (for a 2 bit D/A converter ii)0110(for a 4 bit DAC) iii) 10111100 (for a 8 bit DAC)	Evaluate	5
6	If the analog signal Va is +4.129 V in the example 10.4, find the equivalent digital number	Evaluate	5

7	A dual slope uses a 16 bit counter and a 4 MHz clock rate. The maximum input voltage is +10V. The maximum integrator output voltage should be -8V when the counter has cycled through 2n counts. The capacitor used in the integrator is 0.1µf. Find the value of the resistor R of the integrator	Evaluate	5
8	How many levels are possible in a two bit DAC what is its resolution if the output range is 0 to 3V	Evaluate	5
9	Sketch the circuit diagram of a 6 bit inverted R-2R ladder DAC	Evaluate	5
10	Find V(1)=5V what is the maximum output voltage	Evaluate	5
11	Calculate what is the conversion time of a 10 bit successive approximation A/D converter if its 6.85V	Evaluate	5
12	Explain the limitations of three terminal regulators.	Evaluate	5
13	Construct neat diagram explain the operation of Dual-Slope ADC.	Evaluate	5
14	Sketch the diagram and explain the operation of Successive approximation type ADC.	Evaluate	5
15	Explain the operation of Flash type ADC with a neat diagram.	Evaluate	5

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