Patent Search

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Abstract:

The present invention relates to a system and method for optimizing VLSI layouts specifically in connected and pyramid networks using deep learning techniques. As complexity of VLSI designs increases, traditional optimization methods often fall short in meeting performance metrics such as wire length, power consumption, and constraints. This invention leverages a deep neural network trained on extensive historical design data to predict optimal layout parameters. The system integrates a optimization engine that refines these predictions through advanced techniques, resulting in high-performance, efficient layouts ready for implementation in standar tools. This innovative approach not only enhances the accuracy and speed of VLSI layout optimization but also addresses the evolving needs of the semiconductor in paving the way for future advancements in integrated circuit design. Accompanied Drawing [FIGS. 1-2]

Complete Specification

Description:[001] The present invention relates to the field of Very-Large-Scale Integration (VLSI) design, which is pivotal in the semiconductor and integrated circuit industries. VLSI technology enables the integration of millions or billions of transistors onto a single chip, facilitating the creation of compact and powerful electroni devices. As the complexity of VLSI designs continues to increase, optimizing the layout of these circuits has become a critical task. Efficient layout optimization direc impacts performance metrics such as speed, power consumption, and area utilization.

[002] Traditional approaches to VLSI layout optimization often rely on heuristic algorithms that may not effectively address the intricacies of modern designs, partic complex topologies such as connected and pyramid networks. These networks present unique challenges due to their specific connectivity patterns and hierarchica structures, necessitating advanced optimization techniques. The limitations of conventional meth , Claims:1. A system for optimizing VLSI layouts in connected a pyramid networks, comprising a deep learning model configured to predict optimal layout parameters based on input design specifications.

2. The system of claim 1, wherein the deep learning model is trained using historical VLSI design data, employing supervised and reinforcement learning techniqu

3. A method for VLSI layout optimization, comprising preprocessing input design parameters, extracting relevant features, and generating layout predictions throu deep learning model.

4. The method of claim 3, further comprising refining the generated layout predictions using an optimization engine that applies local wire length minimization ar congestion reduction techniques.

5. A computer-readable medium storing instructions for executing the method of claim 3, enabling the optimization of VLSI layouts for connected and pyramid ne

6. The system of claim 1, wherein the output module generates optimized layouts in industry-standard formats compati

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