Patent Search

Invention Title	VLSI LAYOUT USING REDUNDANT NODES TO INCREASE THE RELIABILITY
Publication Number	08/2023
Publication Date	24/02/2023
Publication Type	INA
Application Number	202341008225
Application Filing Date	08/02/2023
Priority Number	
Priority Country	
Priority Date	
Field Of Invention	PHYSICS
Classification (IPC)	G06F0030394000, G01C0021340000, G06F0030390000, H04L0045280000, G05B0009030000

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Abstract:

[030] The present invention particularly relates to the VLSI layout using redundant nodes to increase the reliability. The invention provides a method for locating a sin first path connecting two elements, deciding whether an alternative route (other than a redundant via) is available for connecting the two elements, and inserting a s into the available alternate route. More redundancy is offered by combining the first and second pathways than by only inserting a redundant via. More crucially, such pathways offer redundancy in cases where congestion makes it impossible to put a redundant through next to the single via. If all of the extra vias utilised to create th way can be declared redundant, one embodiment of the process additionally entails deleting the single through and any unnecessary wire segments. Accompanied D 1]

Complete Specification

Description:[001] The present invention relates to the very large-scale integration (VLSI). The invention more particularly relates to the VLSI layout using redundant n increase the reliability.

BACKGROUND OF THE INVENTION

[002] The following description provides the information that may be useful in understanding the present invention. It is not an admission that any of the informati provided herein is prior art or relevant to the presently claimed invention, or that any publication specifically or implicitly referenced is prior art.

[003] It has been harder to make very large-scale integrated circuits (VLSI) with reliability as their physical dimensions continue to get smaller. The smaller the featu widths and the space between features, the more susceptible a VLSI design is to random flaws. Additionally, it is particularly undesirable to have single vias (i.e., inte couplings through a single via). A single via is particularly likely to result in chip failure from the perspective of random-defect yield because a spot defect falling on a via will result in an open circuit. From the standpoint of systematic yield, if vias are challenging to produce in a certain process, a poorly made single via could result circuit open or a connection that is very resistive, which might cause a circuit to malfunction due to timing issues. Via yield issues are very vulnerable to new produc procedures.

[004] By adding redundant vias, either as a part of the routing stage or as a separate post-routing step, one method for improving the quality of via connections in a scheme is to add redundant vias. In order to add a redundant via between the metal planes, post-routing methods are disclosed in prior art. These methods use a l search to locate a free space in a wiring track close to the single via in one or both metal planes. Other techniques for establishing redundant vias may involve movi wires next to the single via to make room for a redundant via to be put in the next wiring track. Also prior art provides a method for including non-tree routing in a V

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