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Application Details	
APPLICATION NUMBER	202141020084
APPLICATION TYPE	ORDINARY APPLICATION
DATE OF FILING	02/05/2021
APPLICANT NAME	1 . Dr.P.Ashok Babu 2 . Dr.T.Muthumanickam 3 . Dr.Suresh Kumar Pittala 4 . Mr.Gaddam Sunil Kumar 5 . Dr.Sudip Mandal 6 . Mr.Tarun Jaiswal 7 . Mr.G.Ravi 8 . Dr D.Thirumal Reddy 9 . Mr.Pijush Dutta 10 . Mr.Shaik Karimullah
TITLE OF INVENTION	A NOVEL METHOD AND SYSTEM FOR DESIGNING VLSI CIRCUITRY TO OPTIMIZE THE INTEGRATED CIRCUIT OPERATION
FIELD OF INVENTION	ELECTRONICS
E-MAIL (As Per Record)	harishvats@live.com
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E-MAIL (UPDATED Online)	
PRIORITY DATE	
REQUEST FOR EXAMINATION DATE	--
PUBLICATION DATE (U/S 11A)	07/05/2021

Application Status	
APPLICATION STATUS	Awaiting Request for Examination

View Documents

➡ Filed ➡ Published ➡ RQ Filed ➡ Under Examination ➡ Disposed

In case of any discrepancy in status, kindly contact ipo-helpdesk@nic.in

Patent Search

Invention Title	A NOVEL METHOD AND SYSTEM FOR DESIGNING VLSI CIRCUITRY TO OPTIMIZE THE INTEGRATED CIRCUIT OPERATION
Publication Number	19/2021
Publication Date	07/05/2021
Publication Type	INA
Application Number	202141020084
Application Filing Date	02/05/2021
Priority Number	
Priority Country	
Priority Date	
Field Of Invention	ELECTRONICS
Classification (IPC)	G06F0030394000, G06F0030392000, H01S0005100000, H01S0005020000, H01L0023000000

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Abstract:

ABSTRACT A NOVEL METHOD & SYSTEM FOR DESIGNING VLSI CIRCUITRY TO OPTIMIZE THE INTEGRATED CIRCUIT OPERATION [031] The present invention discloses a system for designing VLSI circuitry. The system includes, but not limited to a top semiconductor layer constructed with a material with a higher resistivity and a higher transparency properties; a routing area having a plurality of component tiles positioned thereon; a means configured for reconfiguring the component tiles, enabling the design into a maximal component tiles and a maximal space tiles; and a processor for providing the instructions while designing and constructing the top semiconductor layer, the routing area, the component tiles and maximal space tiles. Accompanied Drawing [FIGS. 1 & 2]

Complete Specification

Claims:We Claim:

1. A system for constructing a circuitry of a very large scale integration (VLSI), comprising:
a top semiconductor layer constructed with a material with a higher resistivity and a higher transparency properties;
a routing area having a plurality of component tiles positioned thereon;
a means configured for reconfiguring the component tiles, enabling the design into a maximal component tiles and a maximal space tiles; and
a processor for providing the instructions while designing and constructing the top semiconductor layer, the routing area, the component tiles and maximal space tiles.
2. The system as claimed in claim 1, wherein the processor is configured to monitor and control the VLSI designing environment to optimize the integrated circuit operation.
3. The system as claimed in claim 1, wherein the VLSI designing environment includes temperature monitoring at a plurality of locations on the integrated circuit, monitoring power supplied to the integrated circuit, monitoring clock frequency of the integrated circuit.
4. The system as claimed in claim 1, wherein the top semiconductor layer is further attached with an upper layer to the top of the VLSI structure.
5. The system as claimed in claim 4, wherein the upper layer includes a mounting location for at least one of a photonic devices or an electronic devices.
6. The system as claimed in claim 1, wherein the means further for identifying a first one of the plurality of maximal component tiles as a starting tile S and for identifying a second one of said plurality of maximal component tiles as a destination tile T.
7. The system as claimed in claim 1, wherein the means further for determining a low cost path between said starting tile S and said destination tile T

View Application Status

"**FORM 1** THE PATENTS ACT 1970 (39 of 1970) and THE PATENTS RULES, 2003 **APPLICATION FOR GRANT OF PATENT** (See section 7, 54 and 135 and sub-rule (1) of rule 20)	(FOR OFFICE USE ONLY)

	Application No.	
	Filing date:	
	Amount of Fee paid:	
	CBR No:	
	Signature:	
1. APPLICANT'S REFERENCE / IDENTIFICATION NO. (AS ALLOTTED BY OFFICE)		

2. TYPE OF APPLICATION [Please tick (✓) at the appropriate category]

Ordinary (✓)		Convention ( )		PCT-NP ( )	
Divisional ( )	Patent of Addition ( )	Divisional ( )	Patent of Addition ( )	Divisional ( )	Patent of Addition ( )

3A. APPLICANT(S)

Name in Full	Nationality	Country of Residence	Address of the Applicant
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3. Dr.Suresh Kumar Pittala	INDIAN	India	Associate Professor, Department of Electronics and Communication Engineering, R.V.R. & J.C. College of Engineering (Autonomous), Chandramoulipuram, Chowdavaram, Guntur, Andhra Pradesh, India. Pin Code: 522019
4. Mr.Gaddam Sunil Kumar	INDIAN	India	Assistant Professor, Department of Electronics and Communication

			Engineering, St.Peter's Engineering College, Maisammaguda, Hyderabad, Telangana, India. Pin Code:500100
5. Dr.Sudip Mandal	INDIAN	India	Assistant Professor, Department of Electronics and Communication Engineering, Jalpaiguri Government Engineering College, Jalpaiguri, West Bengal, India. Pin Code:735102
6. Mr.Tarun Jaiswal	INDIAN	India	Research Scholar, Department of Computer Application, National Institute of Technology (NITRR), Raipur, Chhattisgarh, India. Pin Code:492010
7. Mr.G.Ravi	INDIAN	India	Assistant Professor, Department of Electronics and Communication Engineering, Visvesvaraya College of Engineering and Technology, M. P. Patelguda Village, Ibrahimpatnam Mandal, Ranga Reddy (District), Telangana, India. Pin Code:501510
8. Dr D.Thirumal Reddy	INDIAN	India	Professor, Department of ECE, Sri Indu College of Engineering and Technology, Hyderabad, Telangana, India. Pin Code:501510
9. Mr.Pijush Dutta	INDIAN	India	Assistant Professor & Head of the Department, Department of ECE, Global Institute of Management and Technology, Palpara More, NH-34, Krishnanagar, Nadia, West Bengal, India. Pin Code:741102
10. Mr.Shaik Karimullah	INDIAN	India	Assistant Professor, Department of ECE, Annamacharya Institute of Technology and Sciences, Rajampet, Kadapa, Andhra Pradesh, India. Pin Code:516126

3B. CATEGORY OF APPLICANT [Please tick (✓) at the appropriate category]			
Natural Person (✓)	Other than Natural Person		
	Small Entity ( )	Startup ()	Others ()

4. INVENTOR(S) [Please tick (✓) at the appropriate category]		
Are all the inventor(s) same as the applicant(s) named above?	Yes (✓)	No ()

If "No", furnish the details of the inventor(s)

Name in Full	Nationality	Country of Residence	Address of the Inventor
Same as Applicant			

5. TITLE OF THE INVENTION

A NOVEL METHOD & SYSTEM FOR DESIGNING VLSI CIRCUITRY TO OPTIMIZE THE

INTEGRATED CIRCUIT OPERATION		
6. AUTHORISED REGISTERED PATENT AGENT(S)	IN/PA No.	
	Name	
	Mobile No.	
7. ADDRESS FOR SERVICE OF APPLICANT IN INDIA	Name	Dr.P.Ashok Babu
	Postal Address	Professor and Head, Department of Electronics and Communication Engineering, Institute of Aeronautical Engineering, Hyderabad, Telangana, India. Pin Code:500043
	Telephone No.	
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	Fax No.	
	E-mail ID	harishvats@live.com; harishvats2050@gmail.com;

~~8. IN CASE OF APPLICATION CLAIMING PRIORITY OF APPLICATION FILED IN CONVENTION COUNTRY, PARTICULARS OF CONVENTION APPLICATION~~

~~Country~~	~~Application Number~~	~~Filing date~~	~~Name of the applicant~~	~~Title of the invention~~	~~IPC (as classified in the convention country)~~

~~9. IN CASE OF PCT NATIONAL PHASE APPLICATION, PARTICULARS OF INTERNATIONAL APPLICATION FILED UNDER PATENT CO-OPERATION TREATY (PCT)~~

~~International application number~~	~~International filing date~~

~~10. IN CASE OF DIVISIONAL APPLICATION FILED UNDER SECTION 16, PARTICULARS OF ORIGINAL (FIRST) APPLICATION~~

~~Original (first) application No.~~	~~Date of filing of original (first) application~~

~~11. IN CASE OF PATENT OF ADDITION FILED UNDER SECTION 54, PARTICULARS OF MAIN APPLICATION OR PATENT~~

~~Main application/patent No.~~	~~Date of filing of main application~~

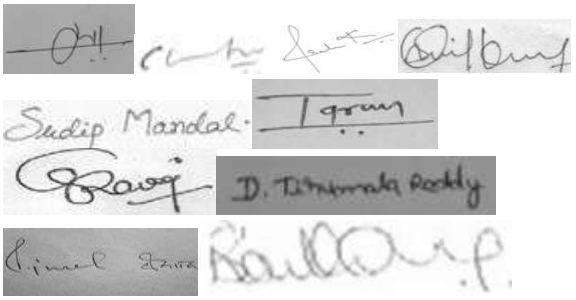
12. DECLARATIONS

(i) Declaration by the inventor(s)

(**In case the applicant is an assignee**: the inventor(s) may sign herein below or the applicant may upload the assignment or enclose the assignment with this application for patent or send the assignment by post/electronic transmission duly authenticated within the prescribed period).

I/We, the above named inventor(s) is/are the true & first inventor(s) for this Invention and declare that the applicant(s) herein is/are my/our assignee or legal representative.

(a)Date 02/05/2021

(b)Name	(c)Signature
1. Dr.P.Ashok Babu 2. Dr.T.Muthumanickam 3. Dr.Suresh Kumar Pittala 4. Mr.Gaddam Sunil Kumar 5. Dr.Sudip Mandal 6. Mr.Tarun Jaiswal 7. Mr.G.Ravi 8. Dr D.Thirumal Reddy 9. Mr.Pijush Dutta 10. Mr.Shaik Karimullah	

~~**(ii) Declaration by the applicant(s) in the convention country**~~

~~**(In case the applicant in India is different than the applicant in the convention country:** the applicant in the convention country may sign herein below or applicant in India may upload the assignment from the applicant in the convention country or enclose the said assignment with this application for patent or send the assignment by post/electronic transmission duly authenticated within the prescribed period)~~

~~I/We, the applicant(s) in the convention country declare that the applicant(s) herein is/are my/our assignee or legal representative.~~

~~(a) Date~~

~~(b) Signature(s)~~

(c) ~~Name(s) of the signatory~~

(iii) Declaration by the applicant(s)

I/We the applicant(s) hereby declare(s) that: -

- ☐ ~~I am/~~ We are in possession of the above-mentioned invention.
- ☐ The ~~provisional~~/complete specification relating to the invention is filed with this application.
- ☐ ~~The invention as disclosed in the specification uses the biological material from India and the necessary permission from the competent authority shall be submitted by me/us before the grant of patent to me/us.~~
- ☐ There is no lawful ground of objection(s) to the grant of the Patent to me/us.
- ☐ ~~I am~~/we are the true & first inventor(s).
- ☐ ~~I am/we are the assignee or legal representative of true & first inventor(s).~~
- ☐ ~~The application or each of the applications, particulars of which are given in Paragraph-8, was the first application in convention country/countries in respect of my/our invention(s).~~
- ☐ ~~I/We claim the priority from the above mentioned application(s) filed in convention country/countries and state that no application for protection in respect of the invention had been made in a convention country before that date by me/us or by any person from which I/We derive the title.~~
- ☐ ~~My/our application in India is based on international application under Patent Cooperation Treaty (PCT) as mentioned in Paragraph-9.~~
- ☐ ~~The application is divided out of my /our application particulars of which is given inParagraph-10 and pray that this application may be treated as deemed to have been filed on DD/MM/YYYY under section 16 of the Act.~~
- ☐ ~~The said invention is an improvement in or modification of the invention particulars of which are given in Paragraph-11.~~

13. FOLLOWING ARE THE ATTACHMENTS WITH THE APPLICATION

(a) Form 2

Item	Details	Fee	Remarks
Complete/ ~~Provisional~~ specification)#	No. of pages : 17		
No. of Claim(s)	No. of claims : 07 No. of pages: 02		
Abstract	No. of pages: 01		
No. of Drawing(s)	No. of drawings: 02 No. of pages: 01		

In case of a complete specification, if the applicant desires to adopt the drawings filed with his provisional specification as the drawings or part of the drawings for the complete specification under rule 13(4), the number of such pages filed with the provisional specification are required to be mentioned here.

(b) Complete specification (in conformation with the international application)/as amended before the International Preliminary Examination Authority (IPEA), as applicable (2 copies).

(c) Sequence listing in electronic form

(d) Drawings (in conformation with the international application)/as amended before the International Preliminary Examination Authority (IPEA), as applicable (2 copies).

(e) Priority document(s) or a request to retrieve the priority document(s) from DAS (Digital Access Service) if the applicant had already requested the office of first filing to make the priority document(s) available to DAS.

(f) Translation of priority document/Specification/International Search Report/International Preliminary Report on Patentability.

(g) Statement and Undertaking on Form 3

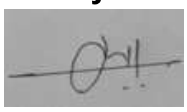
(h) Declaration of Inventorship on Form 5

(i)Power of Authority

(j)**Total fee ₹…….in Cash/ Banker's Cheque /Bank Draft bearing No..... Date on……. Bank.**

I/We hereby declare that to the best of my/our knowledge, information and belief the fact and matters slated herein are correct and I/We request that a patent may be granted to me/us for the said invention.

Dated this 2nd day of May, 2021

Signature: 

Name: Dr.P.Ashok Babu et. al.

To,
The Controller of Patents
The Patent Office, at Chennai

Note: -

* Repeat boxes in case of more than one entry.
* To be signed by the applicant(s) or by authorized registered patent agent otherwise where mentioned.
* Tick ()/cross (x) whichever is applicable/not applicable in declaration in paragraph-12.
* Name of the inventor and applicant should be given in full, family name in the beginning.
* Strike out the portion which is/are not applicable.
* For fee: See First Schedule";