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Patent Search

Invention Title	SYSTEM AND METHOD TO IMPROVE PERFORMANCE OF AMPLIFIERS USING BIAS CURRENT
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Field Of Invention	MICRO BIOLOGY
Classification (IPC)	C12Q1/6869
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Abstract:

Exemplary embodiments of the present disclosure are directed towards a system for improving the performance of amplifiers using bias current, comprising: a comp 102 comprises a simulation module 104 configured to design an architecture of an amplifier using an active comb filter to remove the selected frequencies of various whereby the active comb filter is based on only operational transconductance amplifiers (OTAs) and capacitors that makes it suitable for implementation of monolith circuits (ICs), the computing device 102 configured to perform simulation using cadence virtuoso analog design environment in CMOS technology to examine the effe current for different ECG performance parameters. FIG. 1

Complete Specification

1. A system for improving the performance of amplifiers using bias current, comprising:

a computing device 102 comprises a simulation module 104 configured to design an architecture of an amplifier using an active comb filter to remove the selected frequencies of various signals, whereby the active comb filter is based on only operational transconductance amplifiers (OTAs) and capacitors that makes it suitable implementation of monolithic integrated circuits (ICs), the computing device 102 configured to perform simulation using cadence virtuoso analog design environme CMOS technology to examine the effect of bias current for different ECG performance parameters;

2. The system of claim 1, wherein the computing device 102 comprises simulation module 104 configured to test the workability of the analog circuit for different signals of 60, 180, 300, and 420 Hz as in ECG signal.

- The system of claim 1, wherein the simulation module 104 configured to control the bias current of this analog circuit by controlling the voltage of the OTA. 3.
- The system of claim 1, wherein the active comb filter comprises a resistance (??) and an inductance (??) are primarily dependent on the bias current of respective 4.

5 The system of claim 1 wherein the operational transconductance amplifiers comprises of NMOS transistors of 0.45 W (um) and 0.18 L (um)

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Claims:What is claimed is:



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Application Details			
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APPLICATION TYPE	ORDINARY APPLICATION		
DATE OF FILING	21/10/2019		
APPLICANT NAME	MTE Industries Pvt Ltd.		
TITLE OF INVENTION	SYSTEM AND METHOD TO IMPROVE PERFORMANCE OF AMPLIFIERS USING BIAS CURRENT		
FIELD OF INVENTION	ELECTRICAL		
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ADDITIONAL-EMAIL (As Per Record)	patentagent@prometheusip.com		
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APPLICATION STATUS

FER Issued, Reply not Filed

	View Documents
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FORM 1 THE PATENTS ACT, 1970 (39 of 1970) & THE PATENTS RULES, 2003 APPLICATION FOR GRANT OF PATENT [See sections 7,54 & 135 and rule 20(1)]

(FOR OFFICE USE ONLY)

Application No.: Filing Date: Amount of Fee Paid: CBR No.: Signature:

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3. TITLE OF THE INVENTION: SYSTEM AND METHOD TO IMPROVE PERFORMANCE OF AMPLIFIERS USING BIAS CURRENT

4. ADDRESS FOR CORRESPONDENCE OF APPLICANT /

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5. PRIORITY PARTICULARS OF THE APPLICATION(S) FILED IN CONVENTION COUNTRY:

Sr.No. Country Application Number Fili	g Date Name of the Applicant	Tilte of the Invention
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6. PARTICULARS FOR FILING PATENT COOPERATION TREATY (PCT) NATIONAL PHASE APPLICATION:

International Application Number	International Filing Date as Allotted by the Receiving Office	
PCT//		

7. PARTICULARS FOR FILING DIVISIONAL APPLICATION

Original (first) Application Number

Date of Filing of Original (first) Application

8. PARTICULARS FOR FILING PATENT OF ADDITION:

Main Application / Patent Number:	Date of Filing of Main Application
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9. DECLARATIONS:

(i) Declaration by the inventor(s)

I/We, Dr. VALLABHUNI VIJAY, C V SAIKUMARREDDY, CHANDRASHAKER PITTALA, is/are the true & first inventor(s) for this invention and declare that the applicant(s) herein is/are my/our assignee or legal representative.

(a) Date: -----

(b) Signature(s) of the inventor(s):

(c) Name(s): Dr. VALLABHUNI VIJAY, C V SAIKUMARREDDY, CHANDRASHAKER PITTALA,

(ii) Declaration by the applicant(s) in the convention country

I/We, the applicant(s) in the convention country declare that the applicant(s) herein is/are my/our assignee or legal representative.

(a) Date: -----

(b) Signature(s) :

(c) Name(s) of the singnatory: INSTITUTE OF AERONAUTICAL ENGINEERING, Dr. VALLABHUNI VIJAY

(iii) Declaration by the applicant(s)

- The Complete specification relationg to the invention is filed with this application.
- I am/We are, in the possession of the above mentioned invention.

There is no lawful ground of objection to the grant of the Patent to me/us.

10. FOLLOWING ARE THE ATTACHMENTS WITH THE APPLICATION:

Sr.	Document Description	FileName
1	REQUEST FOR EARLY PUBLICATION(FORM-9)	Form 9.pdf
2	REQUEST FOR EXAMINATION (FORM-18)	Form 18.pdf
3	FORM 1	Form 1.pdf
4	COMPLETE SPECIFICATION	Form 2.pdf
5	DRAWINGS	Drawings.pdf
6	STATEMENT OF UNDERTAKING (FORM 3)	Form 3.pdf
7	POWER OF AUTHORITY	POA.pdf
8	DECLARATION OF INVENTORSHIP (FORM 5)	Form 5.pdf

I/We hereby declare that to the best of my/our knowledge, information and belief the fact and matters stated hering are correct and I/We request that a patent may be granted to me/us for the said invention.

Dated this(Final Payment Date): 21 St october . 2019

Laneux

Signature:

Name: PUTTA GANESH (IN/PA/2933)

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