INSTITUTE OF AERONAUTICAL ENGINEERING

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNIACTION ENGINEERING

ASSIGNMENT

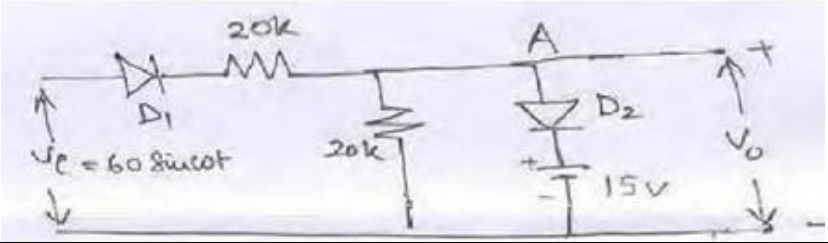
Course Name	:	**PULSE AND DIGITAL CIRCUITS**
Course Code	:	A40415
Class	:	II - B. Tech
Branch	:	ECE
Year	:	2016-17
Course Coordinator	:	Mr. B.Naresh
Course Faculty	:	Mr. B. Naresh, Mrs. P Saritha

OBJECTIVES

To meet the challenge of ensuring excellence in engineering education, the issue of quality needs to be addressed, debated and taken forward in a systematic manner. Accreditation is the principal means of quality assurance in higher education. The major emphasis of accreditation process is to measure the outcomes of the program that is being accredited.

In line with this, Faculty of Institute of Aeronautical Engineering, Hyderabad has taken a lead in incorporating philosophy of outcome based education in the process of problem solving and career development. So, all students of the institute should understand the depth and approach of course to be taught through this question bank, which will enhance learner's learning process.

S.No	QUESTION	Blooms taxonomy level	Course Outcome
	ASSIGNMENT -I **UNIT-I** **LINEAR WAVE SHAPING**		
1	Explain the response of RC High Pass circuit for the following input waveforms A) Step B) Pulse	Understand	1
2	Evaluate the expression for a %tilt of a square wave after passing through a high pass RC Circuit. **(or)** A symmetrical square wave of peak -to-peak amplitude `V' and frequency `f' is applied to a high pass circuit. Show that the percentage tilt is given by P = 1- e(-1/2RC) /1+e(-1/2RC) *100%:	Evaluate	1
3	Explain the operation of RC circuits as Integrators and differentiators for a square wave input With the circuit diagram and waveforms	Understand	1,2
4	Explain the response of RC low pass circuit for exponential input signal	Understand	2
5	Prove that for any periodic input wave form the average level of the steady state output signal from an RC high pass circuit is always zero.	Evaluate	1
6	Explain the response of RL circuit when a step input signal is applied?	Understand	1,2
7	A 1KHz square wave output from an amplifier has rise time tr = 250 ns and tilt = 10%, determine the upper and lower frequencies.	Evaluate	1
8	A 10Hz square wave is fed to an amplifier. Find and sketch the output wave forms under following conditions. The lower 3db frequency is The lower 3db frequency is i. 0.3Hz ii. 3Hz iii. 30Hz	Remember	1
9	A symmetrical square wave whose peak-to-peak amplitude is 2V and whose average value is zero is applied to on RC integrating circuit. The time constant is equals to half -period of the square wave. Find the peak to peak value of the output amplitude.	Remember	2
10	A symmetrical square wave is applied to a HP circuit having R = 20 k and C = 0.05 μ f. If the frequency of input signal is 1kHz and the signal swings	Understand	

	between +0.5V to -0.5V , illustrate the output wave shape and indicate the voltages, also explain what happens if the input signal frequency is reduced to 100 Hz?		1
	UNIT -2 **NON LINEAR WAVE SHAPING**		
1	Prove the clamping circuit theorem	Evaluate	6
2	List the circuits of different types of shunt clippers and explain their operation with the help of their transfer characteristics.	Remember	4
3	Explain positive peak clipping without reference voltage.	Understand	4
4	Explain about positive peak voltage limiters above reference level.	Understand	4
5	Compare series diode clipper and shunt diode clipper.	Evaluate	4
6	What is synchronized clamping? Explain.	Remember	5
7	Analyze the diode comparator circuit. Draw the response of the circuit to a ramp input Vi=lt.	Analyze	6
8	Explain the working of Transistor Clipper with the help of neat Circuit diagram	Understand	4
9	Explain in brief about Practical Clamping?	Understand	5
10	Design the diode shunt clipper that clips the sine wave signal above +5V and below -5V.	Create	5
11	For the clipper circuit shown in figure, the input vi = vi = 60 sin ωt. Find and plot to Scale i. The transfer characteristic indicating slopes and intercepts. ii. Input / output on the same scale. Assume ideal diodes. 	Remember	4
12	Design a diode clamper circuit to clamp the positive peaks of the input signal at zero level. The frequency of the input signal is 500 Hz?	Create	5
13	A 100V peak square wave with an average value of 0V is to be negatively Clamped at 25V. Illustrate the output waveforms?	Understand	5
	UNIT-3 **STEADY STATE SWITCHING CHARACTERISTICS OF A DEVICES & SAMPLING GATES**		
1	Explain the storage and transition times of the diode as a switch.	Understand	7
2	Demonstrate the switching times of BJT by considering charge distribution across the base region. Explain this for cut-off, active and saturation region..	Understand	7
3	Define different Switching times of a transistor with suitable collector current versus time characteristics	Remember	7
4	Explain the temperature sensitivity parameters of a transistor	Understand	7
5	Explain the saturation parameters of a transistor	Understand	7
	ASSIGNMENT-II **STEADY STATE SWITCHING CHARACTERISTICS OF A DEVICES & SAMPLING GATES**		
1	Find the expressions for gain and minimum control voltages of a bidirectional two- diode sampling gate ?	Remember	8
2	Illustrate with neat circuit diagram, the operation of unidirectional sampling gate for multiple inputs.	Understand	8
3	a) Why the sampling gates are called linear gates? (b) Compare the unidirectional and bi-directional sampling gates.	Remember	8
4	Explain the effect of control voltage on gate output of unidirectional sampling gate using diode with some example.	Understand	8
5	Explain the basic principles of sampling gates using series switch and also give the applications of sampling gate.	Understand	7
6	The forward voltage across diode is 0.4 V and forward current through it is 10nA at temperature 27 degree Celsius. For forward voltage of 42V the current through diode becomes twice. Determine the value of I_o.	Evaluate	7

7	Design a high speed common emitter transistor switch operating with two power supplies Vcc=12V and $-V_{BB}$= -10V. the transistor is expected to operate at Ic= 8mA, I_B=0.75mA.The static current gain h_{FE} of the transistor is 30, $_{VBE(sat)}$ = 0.3V, and $R_2=3R_1$.Determine the values of the three resistors Rc, R_1 ,R_2.	Create	7
8	Design the Transistor switch (Inverter) for the following specifications Vin= ±3Vsquare wave, VCC=10V, IC=1mA, hFE=50.Assume Si transistor?	Create	7
	UNIT-IV **MULTIVIBRATORS & TIME BASE GENERATORS**		
1	Define the terms slope error, displacement error and transmission error of time-base signal.	Remember	11
2	Explain the working of a transistor Miller time base generator. With the help of a neat circuit diagram and waveforms	Understand	11
3	Explain how to draw the various waveforms and calculate their volatage levels in an emitter-coupled monostable multi.	Understand	10
4	Solve an expression for slope error (es) for an exponential sweep results when a capacitor is charged from a supply voltageV through a resistor R. If the peak sweep voltage is Vs	Apply	11
5	Design the circuit of a linear current sweep and explain its operation with waveforms. Explain the necessity of generating trapezoidal waveform.	Create	11
6	Explain the operation of Fixed-Bias Bistable multivibrator with circuit diagram and waveforms.	Understand	10
7	Explain the working of a Self bias Bistable multivibrator circuit with the help of waveforms and circuit diagram.	Understand	10
8	Distinguish between unsymmetrical and Symmetrical triggering? Why it is used?	Analyze	10
9	Explain different triggering methods of binary circuits.	Understand	10
10	Design a Schmitt trigger circuit using NPN transistors having hFE(MIN) =60 . VBE cut-off = 0V, VCE(Sat) = 0.2V and VBE(Sat) = 0.7V. Given Vcc=8V and o/p swing = 6V, UTP = 3.5V, LTP = 1.5V, R1 = 10K AND R2 = 2K.Determine Rc1, Rc2 and Re?	Create	10
11	Design a transistor bootstrap ramp generator to provide an output amplitude of 12V over a time period of 2ms. The input signal is a negative going pulse with an amplitude of 5 V, a pulse width of 2ms and the time interval between pulses is 0.5ms. The load resistance is 1K and the ramp is to be linear within 1%. The supply is to be 15V. take hfe(min) = 80.	Create	11
12	Design a Fixed Bias binary by given fallowing specifications, Vcc=Vbb=12V, hfe(min) = 20,Ic(sat)=4mA Assume npn si-Transistors	Create	10
13	Design a Self Bias binary using si transistors. Vcc=6V, hfe(min) =30,Assume appropriate junction voltages for your design?	Create	10
14	The normal self-biased binary uses npn si transistors having worst-case values of Vce(sat)=0.4V, Vbe(sat)=0.8V and zero base to emitter voltage for cutoff. The circuit parameters are Vcc =20V,Rc1=Rc2=4.7kΩ, R1=30 kΩ,R2=15kΩ and Re=390 kΩ a) Find Stable state Currents and Voltages. b) Find the minimum value of hfe required to give the values of part(a) c) As the temperature is increased, what is the maximum value to which Icbo can increase before the condition is reached where neither transistor is OFF.	Remember	10
	UNIT-V **SYNCHRONIZATION AND FREQUENCY DIVISION & LOGIC FAMILIES**		
1	Explain the working of Inverter using circuit diagram?	Understand	15
2	Explain the operation of diode - resistor logic AND & OR gate using circuit diagram	Understand	15
3	What do you mean by a relaxation circuit? Give a few examples of relaxation circuits.	Understand	
4	Explain sine wave frequency division using a sweep circuit with the help of neat waveforms	Evaluate	13
5	Explain the method of pulse synchronization of relaxation devices, with examples.	Understand	13
6	Explain the frequency division in monostable multivibrator with the help of	Evaluate	13

	circuit diagram & waveforms?		
7	Define the terms phase delay and phase jitter. What is the condition to be met for pulse synchronization?	Remember	13
8	Compare TTL and RTL logic and Draw the Transistor logic NAND gate and explain its operation.	Understand	
9	The relaxation oscillator when running freely generates output sweep amplitude of 100V and frequency 1kHz. Synchronizing pulses are applied such that at each pulse the breakdown voltage is lowered by 20V. Over what frequency range the synchronizing pulse frequency may be varied if 1:1 synchronization is to result?	Apply	14
10	Design a transistor inverter circuit (NOT gate) with the following specifications: VCC = VBB = 10V, I_{Csat} = 10mA, h_{femin} = 30. The input is varying between 0 and 10V. Assume typical junction voltages of npn silicon transistor	Create	15

Prepared By: Mr. B. Naresh, Assistant Professor, Department of ECE

Date: 05th December, 2016 **HOD, ECE**