Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC020

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Four Year B.Tech III Semester End Examinations (Regular) - November, 2018

Regulation: IARE – R16

DIGITAL LOGIC DESIGN

Time: 3 Hours **(Common to CSE | IT)** **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Convert **[7M]**
   i)Decimal number 2469 to BCD code and Excess 3 code
   ii)Binary number 1011010 to gray code and octal.
   (b) i)Perform the subtraction using 2's complement (36-84) **[7M]**
   ii) Perform the subtraction using 10's complement (57-96).
2. (a) Differentiate 1's complement and 2's complement addition with example. **[7M]**
   (b) Obtain the hamming code for data 1001 using even parity bits. **[7M]**

UNIT – II

3. (a) State and prove the Demorgan's theorem with suitable example. **[7M]**
   (b) Implement F(x,y,z) = $\sum(1,2,3,4,5,7)$ only using NAND gates. **[7M]**
4. (a) Convert boolean expression F = A + B'C to minterm. **[7M]**
   (b) Simplify F(w,x,y,z) = $\sum(1,3,10) + \sum_d(0,2,8,12)$ and realize using logic gates. **[7M]**

UNIT – III

5. (a) Design a 4-bit parallel Adder-Subtracter circuit and write the drawbacks of the parallel Adder-Subtracter. **[7M]**
   (b) Design a 4×1 multiplexer. Using this, implement 16×1 multiplexer. **[7M]**
6. (a) Draw and explain 4-bit carry-look ahead adder with expressions. **[7M]**
   (b) Explain the design procedure for combinational logic circuit with an example. **[7M]**

UNIT – IV

7. (a) Explain a D latch in detail and implement a master-slave D flipflop. **[7M]**
   (b) Design a Mod-8 synchronous counter using T flipflop. **[7M]**

8. (a) Explain the characteristic table of T and D flipflop and convert a D flipflop to T flipflop. **[7M]**

   (b) Design a parallel input left/right shift serial output register. **[7M]**

UNIT – V

9. (a) Design a BCD to 2421 code converter using suitable PAL. **[7M]**

   (b) Using PROM realize the following expressions $F_1(\text{ABC}) = \sum(0,3,4,5,6)$ and $F_2(\text{ABC}) = \sum(1,3,5,7)$. **[7M]**

10. (a) Implement the circuit with PLA $\text{F(ABCD)} = \sum (0,1,3,5,7,9,11,13)$. **[7M]**

    (b) Explain about types of memories, Moore and Melay machines with examples. **[7M]**

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