Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC008

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

B.Tech V Semester End Examinations (Supplementary) - January, 2019

Regulation: IARE – R16

INTEGRATED CIRCUITS APPLICATIONS

Time: 3 Hours **(Common to ECE | EEE)** **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Derive the expression for Q Point, A, Z_I and Z_0 of a dual input balanced output differential amplifier. **[7M]**

   (b) Determine the output voltage of the differential amplifier having input Voltages V_1=1mV and V_2=2 mV. The amplifier has a differential gain of 5000 and CMRR 1000. **[7M]**

2. (a) Explain the working principle of a BJT differential amplifier with active load. **[7M]**

   (b) An Op - amp has a slew rate of 1.5V/µs. What is the maximum frequency of an output sinusoid of peak value 10 V at which the distortion sets in due to the slew rate limitation? **[7M]**

UNIT – II

3. (a) With the help of neat diagrams explain the operation of Schmitt Trigger using IC741. **[7M]**

   (b) In the following Figure 1, R_1 = 10 kΩ, R_f = 100kΩ, v_i = 1V. A load of 25 kΩ is connected to the output terminal. Calculate (i) i_1 (ii) v_0 (iii)i_L (iv) Total current i_0 into the output pin. **[7M]**

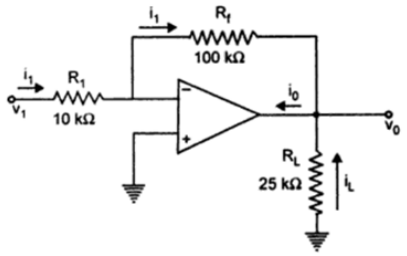

Figure 1

4. (a) Draw the circuit using Op-amp as instrumentation amplifier and explain its working function. **[7M]**

   (b) In the given circuit shown in Figure 2, let R_1 =5 kΩ, R_f = 20 kΩ and v_i =1V. A load resistor of 5 kΩ is connected to the output terminal. Calculate **[7M]**
   (i) v_0 (ii) A_{CL} (iii)i_L (iv) Total current i_0 indicating proper direction of flow.

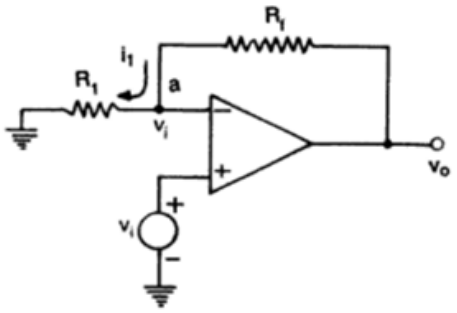

Figure 2

UNIT – III

5. (a) Draw the block diagram of Phase Locked Loop(PLL) and briefly explain about each block in PLL. **[7M]**

   (b) Design a wide Band Pass Filter having fl = 400 Hz, fh = 2 kHz and pass band gain of 4. Find the value of Q of the filter. **[7M]**

6. (a) With the help of circuit diagrams and waveform, explain the working of 555 Timer as Astable multivibrator and derive an expression for frequency. **[7M]**

   (b) Design a Second order Butterworth Low pass filter having upper cut off frequency 2 KHz. Assume necessary data. **[7M]**

UNIT – IV

7. (a) What output voltage would be produced by a D/A converter whose output range is 0 to 10 V and whose input binary number is **[7M]**

   (i) 10 for a 2-bit D/A Converter (ii) 0110 for a 4-bit D/A Converter

   (iii) 10111100 for an 8-bit D/A Converter

   (b) With the help of neat circuit diagram and waveform explain the operation of Dual Slope ADC. **[7M]**

8. (a) Explain voltage mode and current mode operations of R-2R ladder type DAC. **[7M]**

   (b) A Dual slope ADC uses a 16-bit counter and a 4 MHz clock rate. The maximum input voltage range is +10 V. The maximum integrator output voltage should be -8V when the counter has cycled through 2^n counts. The capacitor used in the integrator is 0.1µF. Find the value of the resistor R of the integrator. **[7M]**

UNIT – V

9. (a) What is a carry look ahead adder? Design and implement carry look ahead adder using logical gates. **[7M]**

   (b) Implement the 4-bit, 8-state Johnson counter using 74x194 and draw the corresponding timing diagram. **[7M]**

10. (a) Compare synchronous and asynchronous counters. Design 4-bit synchronous counter using T-flip-flops. **[7M]**

    (b) Implement the parallel input to serial output shift register using 74x163 and 74x166. **[7M]**

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