INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

B.Tech V Semester End Examinations (Regular) - November, 2018

Regulation: IARE – R16

INTEGRATED CIRCUITS APPLICATIONS

Time: 3 Hours   (Common to ECE | EEE)   Max Marks: 70

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Define CMRR and derive the expression for CMRR. **[7M]**

   (b) For a dual input, balanced output differential amplifier, $R_C = 2.2k\Omega$, $R_E = 4.7$ kΩ, $R_{S1} = R_{S2} = 50\Omega$. The supply voltages are ± 10 V. the h_{fe} for the transistor is 50. Assume silicon transistors and $h_{ie} = 1k\Omega$. Determine the operating point values, differential mode gain, common mode gain and CMRR. **[7M]**

2. (a) What is Input Bias Current and explain how can it be reduced? **[7M]**

   (b) With the help of neat diagrams explain about pole zero compensation technique. **[7M]**

UNIT – II

3. (a) Explain the operation of Log Amplifier using IC741. **[7M]**

   (b) Design an Op-amp circuit to give an output $V_O = - (3V_1+2V_2+0.1V_3)$ for $R_f = 10$ kΩassume necessary data for R_1, R_2, R_3. **[7M]**

4. (a) Design a Practical differentiator at 2KHz. Assume necessary data for R_f and C_{in} **[7M]**

   (b) With the help of neat circuit diagram and waveform explain the operation of Monostable Multi-vibrator using IC741. **[7M]**

UNIT – III

5. (a) Draw the 1st order low pass filter using op-amp and derive the expression for higher cut-off frequency. **[7M]**

   (b) Design a wide band reject filter having $f_h = 400$ Hz and $f_l = 2$kHz having pass band gain as 2. Draw the circuit and corresponding frequency response. **[7M]**

6. (a) With the help of circuit diagram and waveform, explain the working of IC 555 Timer as Monostable multivibrator and derive an expression for pulse width. **[7M]**

   (b) Design a Notch filter using Op-Amp at 300 Hz. **[7M]**

UNIT – IV

7. (a) Explain the following types of digital to analog converters with suitable circuit diagrams. **[7M]**
   (i) R-2R Ladder DAC
   (ii) Inverted R-2R DAC

   (b) Draw the circuit diagram for flash type ADC and explain in detail. **[7M]**

8. (a) Explain the types of digital to analog converters with suitable circuit diagrams for Binary Weighted Resistor DAC. **[7M]**

   (b) With a neat block diagram explain in detail about successive approximation type analog to digital converter. **[7M]**

UNIT – V

9. (a) Design a 4-bit ripple carry adder and explain its working function. **[7M]**

   (b) Design a 4-bit synchronous up-down counter using JK flip-flop. **[7M]**

10. (a) With the help of truth table explain about IC74X85. **[7M]**

    (b) Explain the operation of 4 bit serial in seriel out shift register with the help of functional table. **[7M]**

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