COURSE CONTENT

VLSI DESIGN LABORATORY

VII Semester: ECE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AECC54	Core	-	-	3	1.5	30	70	100
Contact Classes: Nil	Tutorial Classes: Nil	Practical Classes: 36				Total Classes: 36		

Prerequisites: Digital System Design

I. COURSE OVERVIEW:

The art of VLSI circuit design is dynamic with advances in process technology and innovations in the electronic design automation (EDA) industry. The objective of this laboratory course is to demonstrate the various stages in VLSI design flow using cadence software. Hands on training on logic and circuit simulations of MOSFETS, ring oscillators, multiplexers, analog amplifiers etc are included. The course also covers physical layout of complex logic gates for chip design.

II. COURSE OBJECTIVES:

The students will try to learn:

I. Modern tools for functional level to physical layout with verification at intermediate stages in the VLSI design flow in top-down approach.
II. Design and simulations of analog, digital and mixed circuits for optimum values of area over head, power and time delay.
III. The Chip design through a practical approach using advanced modern tools such as vivado and cadence for front end and back end.

III. COURSE SYLLABUS:

Week - 1: MOSFET

To plot the (i) output characteristics
(ii) Transfer characteristics of an n-channel and p-channel MOSFET.

Week - 2: CMOS INVERTER

To design the static (VTC) and dynamic characteristics and layout of a digital CMOS inverter.

Week - 3: RING OSCILLATOR

To design and plot the output characteristics of a 3 stage ring oscillator using CMOS inverters.

Week - 4: LOGIC GATES

To design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS design style

Week - 5: 4X1 MULTIPLEXER

To design and plot the characteristics of a 4x1 digital multiplexer using pass transistor logic and transmission gate logics

Week - 6: LATCHES

To design and plot the characteristics of a positive and negative latch using multiplexers.

Week - 7: REGISTERS

To design and plot the characteristics of a master-slave positive and negative edge triggered registers based on multiplexers.

Week - 8: DIFFERENTIAL AMPLIFIER

Design and simulation of a simple 5 transistor differential amplifier. Measure gain and Common mode rejection ratio.

Week - 9: MOSFET COMMON SOURCE AMPLIFIER
Analysis of Frequency response of Common source amplifiers using n and p MOSFETs

Week - 10: MOSFET COMMON DRAIN AMPLIFIER
Analysis of Frequency response of Common drain amplifiers using n and p MOSFETs

Week - 11: SINGLE STAGE CASCODE AMPLIFIER
Design and Simulation of Single Stage Cascode Amplifier.

Week - 12: BASIC CURRENT MIRROR, CASCODE CURRENT MIRROR AMPLIFIER
Design and Simulation of Basic Current Mirror, Cascode Current Mirror Amplifier.

Week - 13: Design of NAND/NOR using CNTFET
Design and plot the dynamic characteristics of 2-input NAND/ NOR logic gates using CNTFET.

Week - 14: Design of DIFFERENTIAL AMPLIFIER using FinFET
Analysis of Frequency response of differential amplifiers using FinFET.

IV. TEXT BOOKS

1. Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill Publications, 2002.
2. Allen Holberg, "CMOS Analog Circuit Design" Oxford Publications, 2002.
3. Baker, Li, Boyce, "CMOS Mixed Circuit Design", Wiley Publications, 2002.

V. REFERENCE BOOKS

1. Mohammad Rashid, "Electronic Devices and Circuits", Cengage learning, 1st Edition, 2014.
2. David A. Bell, "Electronic Devices and Circuits", Oxford University Press, 5th Edition, 2009.