INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)
Dundigal - 500 043, Hyderabad, Telangana

COURSE CONTENT

DIGITAL DESIGN THROUGH VERILOG

VII Semester: **ECE**

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AECC49	Elective	3	-	-	3	30	70	100
Contact Classes: 45	Tutorial Classes: Nil	Practical Classes: Nil				Total Classes: 45		

Prerequisites: **Digital System Design**

I. COURSE OVERVIEW:

This course introduces the hardware description language for design and development of digital integrated circuits and field programmable devices. Provides hardware description language elements, synthesizable register transfer logic models in gate level, dataflow, behavioral, switch level modeling of combinational and sequential circuits. Allows to use computer aided design tools at the levels of system design, logic design and IC design.

II.COURSE OBJECTIVE:

The students will try to learn:

I. The fundamental principles of the Verilog hardware descriptive language and its constructs used in synthesizable Register Transfer Level (RTL) design implementation of digital logic systems.
II. The concepts of gate level, behavioral, dataflow and switch level modeling of fundamental digital logic circuits using Verilog hardware description Language.
III. The exposure to various stages of a typical 'state of the art' CAD VLSI tool for simulation, synthesis, place and route, layout and power and clock routing modules.
IV. The analytical skills needed to model finite state machines using Field Programmable Gate Arrays, fault-tolerant high-speed computer arithmetic circuits, built-in self-circuit (BIST).

III. COURSE SYLLABUS

MODULE - I: INTRODUCTION TO VERILOG HDL (09)

Introduction to Verilog, Popularity of Verilog HDL, Module Concept, Module Modeling Styles, Language Elements: Comments, Identifiers, Keywords, Value Set, Data Types, Memory Element, Constant, Parameter, Operators. Dataflow Modeling: Continuous Assignment, Implicit Continuous Assignment, Delays, Design examples using data flow modeling.

MODULE - II: GATE-LEVEL MODELING (09)

Multiple-Input Gates, Gate Delays, Design Examples, User-Defined Primitives: UDP Basics Combinational User-Defined Primitives, Sequential User-Defined Primitives, Combinational Logic Modules: Decoders, Encoders, Multiplexers, Demultiplexers, Magnitude Comparators.

MODULE - III: BEHAVIORAL MODELING (10)

Procedural Constructs, Procedural Assignments, Timing Control, Conditional Statements, Case Statement Design examples using behavioral modeling.

Loop Statements: For Loop, While Loop, Repeat Loop, Forever Loop, Block Statements Procedural Continuous Assignment, Design examples using behavioral modeling.

MODULE - IV: SWITCH LEVEL MODELLING (09)

Basic Transistor Switches, CMOS Switch, Bi – directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets.

MODULE - V: SEQUENTIAL LOGIC (08)

Analysis of Synchronous Sequential Machines, Synthesis of Synchronous Sequential Machines, Analysis of Asynchronous Sequential Machines, Synthesis of Asynchronous Sequential Machines, and Synthesis: Design flow of ASICs and FPGA-Based Systems, Design Environment and Constraints, Logic Synthesis.

IV. TEXT BOOKS:

1. Joseph Cavanagh, "Verilog HDL: Digital Design and Modeling", CRC Press, 1st Edition, 2007.
2. Michael D. Ciletti, "Advanced Digital Design with Verilog HDL", PHI, 2005.
3. Joseph Cavanagh, "Digital Design and Verilog HDL Fundamentals", CRC Press, 1st Edition, 2008.

V. REFERENCE BOOKS:

1. Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic design with Verilog Design", TMH, 2nd Edition, 2010.
2. Sunggu Lee "Advanced Digital Logic Design using Verilog, State Machine & Synthesis for FPGA", Cengage Learning, 2012.
3. Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Edition, 2009.
4. T. R. Padmanabhan and B. Bala Tripura Sundari, "Design through Verilog HDL", Wiley, 2009.
5. Zainalabdien Navabi, "Verilog Digital System Design", TMH, 2nd Edition, 2009.

VI. WEB REFERENCES:

1. https://www.crcpress.com/Verilog-HDL-Digital-Design an Modeling/ Cavanag h/p/book/ 9781420051544
2. https://www.uotechnology.edu.iq
3. https://www.iare.ac.in

VII. E-Text Books:

1. https://www.www.jntubook.com
2. https://www.allaboutcircuits.com
3. https://www.archive.org