INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)
Dundigal - 500 043, Hyderabad, Telangana

COURSE CONTENT

VLSI DESIGN								
VII Semester: ECE								
Course Code	**Category**	**Hours / Week**			**Credits**	**Maximum Marks**		
		L	**T**	**P**	**C**	**CIA**	**SEE**	**Total**
AECC44	Core	3	1	-	4	30	70	100
Contact Classes: 45	**Tutorial Classes: 15**	**Practical Classes: Nil**				**Total Classes: 60**		
Prerequisites: Electronic Devices and Circuits								

I. COURSE OVERVIEW:

This course introduces the students to fabrication techniques, rapid design and implementation of very large scale (VLSI) circuits. Specific topics include: CMOS logic, MOSFET theory, selection of technology and logic, design process, design rules and layout procedure, design aid for layout, rule checking, logic and circuit simulation, timing and testability are the main aspects of this course. The course further gives information on data path subsystems, several PLD's performance parameters and testing approaches for the circuits.

II. COURSE OBJECTIVES:

The students will try to learn:

I. The aspects of hierarchical VLSI design from the metal oxide semiconductor transistor up to the system level, fabrication and testing.
II. The subsystem design incorporating into a VLSI chip with contemporary techniques for achieving high-speed, low-power and low area overhead.
III. Advanced modern tools such as Vivado and Cadence for front end and back end for chip design through a practical approach.

III. COURSE SYLLABUS:

MODULE – I: BASICS OF MOSFETS (09)

Introduction to IC Technology: MOS, PMOS, NMOS, CMOS & BiCMOS; Fabrication Flow; Basic Electrical Properties of MOS and BiCMOS Circuits: Ids-Vds relationships in saturation and ohmic regions, Weak & strong inversion conditions, Threshold voltage concept in MOSFETs, gm, gds, Figure of merit; Pass transistor; NMOS Inverter; Various pull ups; CMOS Inverter analysis and design; Simple form of Bi-CMOS Inverters and it's alternative forms.

MODULE – II: MOS CIRCUIT DESIGN PROCESSES (09)

VLSI Design Flow; MOS Layers; Stick Diagrams; Physical design rules: 2 μm and lambda CMOS design rules for wires, contacts and transistors; Euler's rule for physical design and Layout; Transistors Layout Diagrams for NMOS and CMOS Inverters; Scaling of MOS circuits; Trends & projections in VLSI design & technology CMOS nanotechnology; FINFET; CNTFET.

MODULE – III: BASIC CIRCUIT CONCEPTS AND GATE LEVEL DESIGN (10)

Sheet Resistance and area capacitance of layers; Inverter Time delays; Driving large capacitive loads; Propagation Delays; Wiring capacitances; Fan-in and Fan-out; Choice of layers . VLSI Interconnects; Reliability issues in CMOS VLSI; Latching in VLSI, Electro migration.

Gate Level Design: Series and Parallel equivalent circuits, Complex gates; Switch logic; Transmission gates; Other forms of CMOS logic such as Pseudo –nMOS, dynamic CMOS, clocked CMOS, CMOS domino, n-p CMOS and their comparisons.

MODULE – IV: SUBSYSTEM DESIGN (09)

Data Path Sub Systems: Sub system design; Shifters, Ripple carry, Carry Look Ahead; Carry select Adders; Manchester carry chain; ALUs; Multipliers; Parity generators; Comparators; Zero/one detectors; Asynchronous and Synchronous; Counters Array Subsystems: SRAM, DRAM, ROM, Floating gate concepts and Flash Memories, Serial access Memories, Content Addressable Memories.

MODULE – V:PROGRAMMABLE LOGIC DEVICES AND CMOS TESTING (08)

Programmable Logic Devices: Design Approach – PROM, PLA and PAL; FPGAs; CPLDs; FPGA building block architectures; FPGA interconnect routing procedures; Speed and area tradeoff. Implementation strategies full custom and semi custom design; CMOS Testing; Built-in Self –Test Strategies; Test pattern generation using LFSR.

IV. TEXTBOOKS:

1. A. Pucknell; Kamran Eshraghian; "BASIC VLSI Design;" , Prentice Hall of India; 3rd Edition, 2007, ISBN: 978-81-203-0986-9.
2. R. Jacob Baker; Harry W.LI.; David E.Boyee; "CMOS Circuit Design; Layout and Simulation", Wiley-IEEE Press; USA; 2005. ISBN: 978-0-470-88132-3.
3. Jan Rabaey; Anantha Chandrakasan; B.Nikolic; "Digital Integrated Circuits: A Design Perspective;" Second Phi Learning; 2009. ISBN: 9788120322578.

V. REFERENCE BOOKS:

1. N. Weste; K. Eshraghian; "Principles of CMOS VLSI Design"; Addision Wesley; 2nd Edition, 1993, ISBN: 978-81-317-1942-8.
2. M.J. Smith; "Application Specific Integrated Circuits"; Addisson Wesley; 1st Edition; 1997, ISBN-13: 978-0321602756.
3. John P. Uyemura; "CMOS Logic Circuit Design", Springer; USA; 2007. ISBN: 0-7923-8452-0.

VI. WEB REFERENCES:

1. http://www.ee.iitkgp.ac.in
2. http://www.citchennai.edu.in