Code No: R09220402 **R09** **Set No. 2**

II B.Tech II Semester Examinations,Dec/Jan -2011/2012
ELECTRONIC CIRCUIT ANALYSIS
Common to ICE, E.COMP.E, ETM, EIE, ECE

Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw the circuit of a voltage series feedback circuit and explain it.
   (b) What are the possible amplifiers circuits in any feedback system? Discuss. [8+7]

2. Obtain the expressions for the voltage gain in the low frequency, medium frequency and high frequency ranges in the case of single stage amplifier. [15]

3. (a) Give the two Barkhausen conditions required in order for sinusoidal oscillations to be sustained.
   (b) Draw the circuit diagram of RC phase - shift oscillator and derive the expression for frequency of Oscillations & condition for sustained Oscillations. [5+10]

4. (a) Consider an emitter follower and show that as $Re \rightarrow \infty$ $R_i = h_{ie} + \frac{1+h_{fe}}{h_{oe}}$
   (b) State Miller's theorem and its dual. [7+8]

5. (a) Why two tuned circuits are used in double tuned amplifier?
   (b) What are the advantages of stagger tuned amplifier?
   (c) Why parallel resonance circuits are used in tuned amplifiers? [5+5+5]

6. (a) Draw the FET amplifier equivalent circuit looking into the drain and find its gain & o/p impedance?
   (b) Starting with the definition of g_m and r_d, show that if two identical FETs are connected in parallel, g_m is doubled and r_d is halved since $\mu = r_d g_m$, then μ remains unchanged. [8+7]

7. (a) Derive the expression for the bandwidth of multistage amplifier.
   (b) What are the problems of Direct coupled amplifiers?
   (c) Why RC coupling is popular?
   (d) Why transformer coupling is not used in the initial stage of a multistage amplifier? [5+3+3+4]

8. (a) A single ended class A power amplifier is coupled to an 8Ω load, using a transformer with a turn ratio of 5:1 with a 50V supply the transistor is biased to have a quiscent collector current of 250mA. When a sinusoidal signal is

applied to the base, the collector voltage varies between a maximum of 5V and maximum of 90V. Estimate the efficiency, power output & second - harmonic distortion of this stage.

(b) Discuss how rectification may takes place in a power amplifier? [8+7]

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Code No: R09220402 **R09** **Set No. 4**

II B.Tech II Semester Examinations,Dec/Jan -2011/2012
ELECTRONIC CIRCUIT ANALYSIS
Common to ICE, E.COMP.E, ETM, EIE, ECE

Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) In a colpitts oscillator, $C_1 = 0.2\mu F$ and $C_2 = 0.04\mu F$. If the frequency of oscillation is 10KHz, find the value if Inductor. Also, find the required gain for oscillation.
   (b) Determine the frequency of oscillations in a wien bridge oscillator? [8+7]

2. (a) Explain the Principle of opeartion of direct coupled amplifier and mention its advantages.
   (b) What is the use of transformer coupling in the output stage of multi stage amplifier?
   (c) Why RC coupling is mostly used for voltage amplifier. [8+4+3]

3. For the circuit shown in figure 1, show that
   (a) $(A_{VS})_{\max} = -\frac{h_f}{h_i h_o - h_r h_f}$ if $R_L = \infty$ & $R_S = 0$
   (b) $R_i = \frac{h_i h_o - h_r h_f}{h_o}$ if $R_L = \infty$ [8+7]

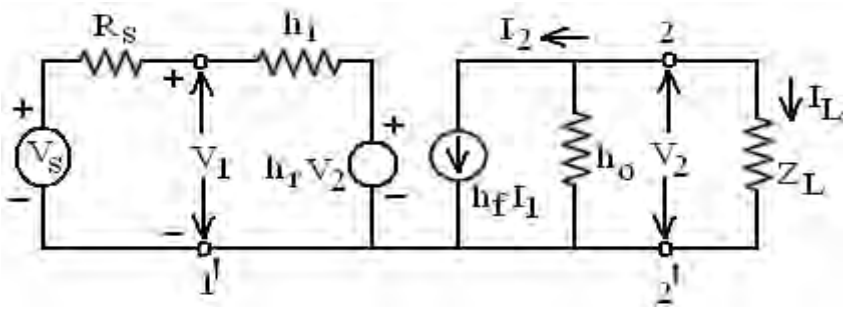

Figure 1:

4. (a) Draw a feedback amplifier in block diagram form and explain each block giving its function.
   (b) Distinguish between regenerative and degenerative feedback in amplifiers.[10+5]

5. (a) The hybrid - π parameters of the transistor at room temperature & for $I_c = 1.3$ mA are $g_m = 50$ mA/V, $r_{b'e} = 1$K, $r_{bb'} = 100\ \Omega$, $r_{b'c} = 4$ MΩ, $r_{ce} = 80$KΩ, $C_c = 3$PF & $C_e = 100$ PF. Using Miller's theorem and the approximate analysis compute the upper 3dB frequency of the current gain and magnitude of the voltage gain at that frequency.

(b) Consider a single - stage CE transistor amplifier with the load resistance R_L shunted by a capacitance C_L. Prove that the internal voltage gain K is $K \approx \frac{-g_m R_L}{1+j\omega(C_C+C_L)R_L}$ [8+7]

6. a) Show the $h_{re} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}}$.
   b) Derive the equation for gain bandwidth product.
   c) Draw and explain a simplified high frequency model [5+5+5]

7. (a) Compare neutralisation and unilaterlisation methods of tuned amplifiers.
   (b) What are the limitations of stagger tuned amplifiers?
   (c) What happen when no. of stages is increased in single tuned cascaded amplifiers? [5+5+5]

8. (a) Show that the maximum conversion efficiency of the idealized class B pus - pull circuit is 78.5%.
   (b) For an ideal class B transistor amplifier the collector supply voltage V_{cc} and the effective load resistance $R_L^1 = (\frac{N_1}{N_2})^2 R_L$ are fixed as the base current excitation is varied. Show that the collector dissipation P_c is zero at no signal, rises as V_m increses and passes through a maximum at $V_m = 2V_{cc}/\pi$. [8+7]

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Code No: R09220402 **R09** **Set No. 1**

II B.Tech II Semester Examinations,Dec/Jan -2011/2012
ELECTRONIC CIRCUIT ANALYSIS
Common to ICE, E.COMP.E, ETM, EIE, ECE

Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) A transistor in CB circuit has the following set of 'h' parameters. $h_{ib} = 20\Omega$, $h_{fb} = 0.98$, $h_{rb} = 3\times10^{-4}$, $h_{ob} = 0.5\times10^{-6}$. Find the values if R_i, R_o, A_i & A_v if $R_s = 600\Omega$ and $R_L = 1.5$ kΩ.
   (b) Draw the CE amplifier with un by passed emitter resistance and derive expression for its R_i & A_v? [8+7]

2. (a) Draw the small signal high frequency equivalent circuit for the source follower and find its voltage gain input and outputimpedances?
   (b) The amplifier stage shown in figure 3 having I_{DSS} = 1mA, V_P = -1V. If the quiescent drain- to - ground voltage is 10V, find R_1? [8+7]

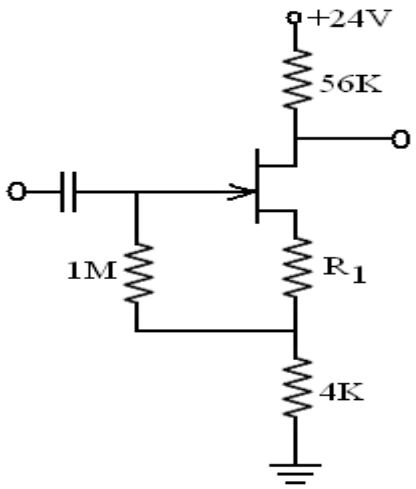

Figure 3:

3. (a) A transistor amplifier in CE configuration is operating at high frequency with the following specifications:
   f_T= 6 MHz, g_m = 0.04 mhos, h_{fe} = 50, $r_{bb'}$ = 100Ω, R_s = 500Ω, C_C = 10 pF, R_L = 100Ω. Compute the voltage gain, upper 3 dB cut off frequency and gain bandwidth product.
   (b) Define unity gain frequency. Obtain the necessary relation using transistor frequency response. [8+7]

4. (a) For the circuit shown in figure 4, find the V_f/V_o & the frequency of oscillations.

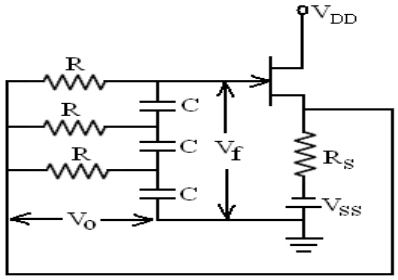

Figure 4:

(b) Draw the colpilts oscillator circuit and explain its working. [8+7]

5. (a) How the frequency response of doubled tuned amplifier depends on degree of coupling between two tank circuits?

   (b) Why the reproducibility of signal is poor at high Q values? [8+7]

6. (a) Explain the origin of crossover distortion. Describe a method to minimize this distortion.

   (b) The power transistor used in the class-B push-pull circuit with $R_2 = 0$ and $-V_{cc} = -20V$ and $R_L^1 = 15\Omega$. If the base voltage is sinusoidal with a peak value of 0.4V. Plot the output collector current. [8+7]

7. (a) Derive the expression for current gain for Darligton pair.

   (b) With a neat sketch explain the principle of operation of cascode amplifier and also expressions for its performance measure. [7+8]

8. (a) Draw the equivalent circuit for a current amplifier and what are the values of R_i & R_o for ideal amplifier?

   (b) For the circuit shown in figure 5, prove that $A_{vf} = \frac{V_o}{V_s} = -\frac{R'}{R}\frac{1}{1+\frac{R'}{R_m}\left(\frac{R_i+R'}{R'}+\frac{R_i}{R}\right)}$. [7+8]

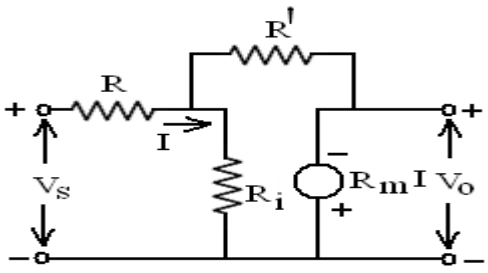

Figure 5:

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Code No: R09220402 **R09** **Set No. 3**

II B.Tech II Semester Examinations,Dec/Jan -2011/2012
ELECTRONIC CIRCUIT ANALYSIS
Common to ICE, E.COMP.E, ETM, EIE, ECE

Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) The open loop gain of an amplifier is 100. What will be the overall gain when a negative feed back of 0.5 is applied to the amplifier?
   (b) What are the different mixing techniques used in any feed back system? Explain.
   (c) State the condition in terms of (1 + Aβ) which a feed back amplifier must satisfy in order to be stable. [4+4+7]

2. (a) How the need of high input impedance can be fullfilted using two CC configuration?
   (b) Find the voltage gain A_{VS} of the amplifier shown in figure 6. Assume h_{ie}=1kΩ, h_{re}=10^{-4}, h_{fe}=50, h_{oe}=10^{-4}A/V. [7+8]

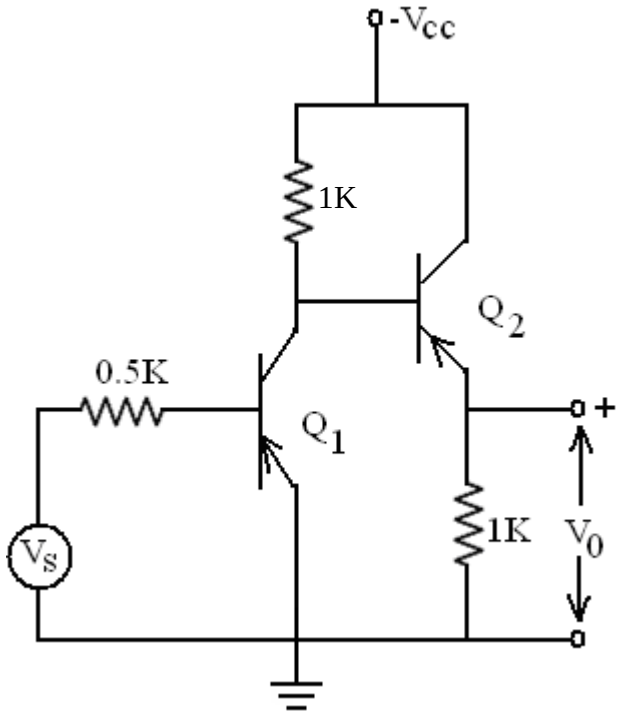

Figure 6:

3. (a) Derive the equation for the lower 3dB frequency of CE configuration.
   (b) Draw the hybrid- Π model of common emitter configuration and describe each component in the Π-model. [7+8]

4. (a) What is class B amplifier? Why is it employed? Give its circuits, design equations, characteristics & limitations.

   (b) A transformer coupled class A large signal amplifier has maximum and minimum values of collector to emitter voltage of 25V and 2.5V. Determine its collector efficiency. [10+5]

5. (a) Draw the equivalent circuit of double tuned amplifier and derive the expression for gain at resonance.

   (b) Derive the expression for effective bandwidth of cascaded tuned amplifier. [8+7]

6. (a) Derive an expression for voltage gain of a common source FET amplifier with and without source resistance included in the circuit.

   (b) Calculate the voltage gain of the FET amplifier shown in the figure 7, assuming blocking capacitor to be large $g_m = 4$ mA/V and $r_d = 5$K. [8+7]

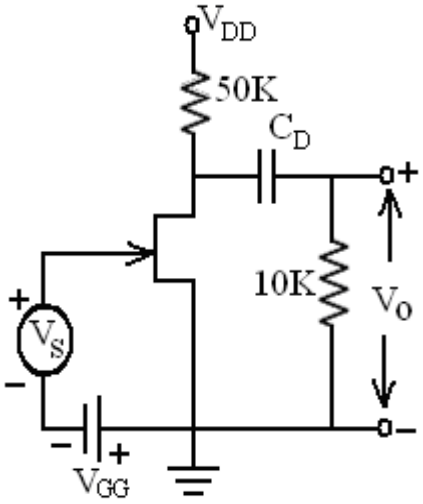

Figure 7:

7. (a) For a common Emitter configuration, what is the maximum value of R_L for which R_i differs by not more than 10% of its value at $R_L = 0$?

   (b) For the circuit shown in figure 8, estimate A_V and R_i. Assume $\frac{1}{h_{oe}}$ is large compared with load seen by the transistor. All capacitors have negiligible reactance at the test frequency, $h_{ie} = 1k\Omega$, $h_{fe} = 99$, h_{re} is negligible. [7+8]

8. Design a phase - shift oscillator to operate at a frequency of 5KHz. use a MOSFET with $\mu = 55$ and $r_d = 5.5$K. The phase - shift network is not to load down the amplifier.

   (a) Find the minimum value of the drain - circuit resistance for which the circuit will oscillate?

   (b) Choose reasonable value of R and find C. [8+7]

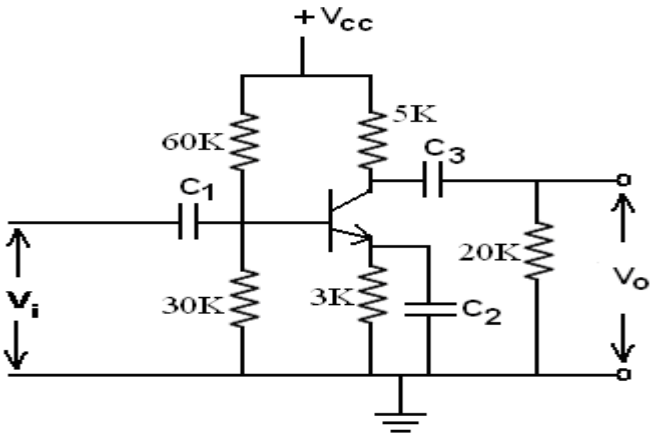

Figure 8:

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R09

Code No: R09220402

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B. Tech II Year - II Semester Examinations, November/December, 2012
ELECTRONIC CIRCUIT ANALYSIS
(COMMON TO ECE, ETM, ICE, E.COMP.E, EIE)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) State Miller's Theorem.
b) Derive the expressions for the Voltage gain, input resistance and output resistance of common collector circuit, using simplified Hybrid Model. [5+10]

2. Two BJT CE amplifiers in self biasing configuration are connected in cascade. The following are the parameters of each circuit:
The biasing resistors are R1 = 10KΩ; R2 = 5KΩ; Collector resistor Rc = 2KΩ; Emitter Resistor Re=2KΩ. h_{ie}=1KΩ; h_{fe}=100. Neglect the effect of h_{oe}.
Calculate the Voltage gain, input impedance and output impedance of the above cascade. [15]

3.a) Draw the Hybrid-π model for a common emitter transistor and explain.
b) Explain about Gain-Bandwidth Product of an amplifier. [10+5]

4.a) Draw and explain the small signal model of a MOS amplifier.
b) Derive the expression for the voltage gain of a MOS-Source Follower. [7+8]

5.a) Explain and justify the effect of Nagative feed back on the characteristics of an amplifier.
b) An amplifier with open loop gain of 2000±150 is available. It is necessary to have the amplifier whose voltage gain varies by not more than ±0.2%. Calculate the feedback factor β, and the gain of the amplifier with feedback. [10+5]

6. Derive the expression for the frequency of oscillations of a BJT-RC Phase shift Oscillator. [15]

7.a) Derive the expression for the efficiency of a direct coupled Class-A amplifier.
b) What is crossover distortion? Explain. [10+5]

8. Write notes on the following:
a) Stagger Tuning b) Single Tuned and Double Tuned Amplifiers. [7+8]

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CODE NO: R09220402 | R09 | SET No - 1

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011
ELECTRONIC CIRCUIT ANALYSIS
(Common to Electronics & Communication Systems, Electronics & Computer Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics, Instrumentation & Control Engineering)

Time: 3hours **Max. Marks: 75**

Answer any FIVE questions
All Questions Carry Equal Marks

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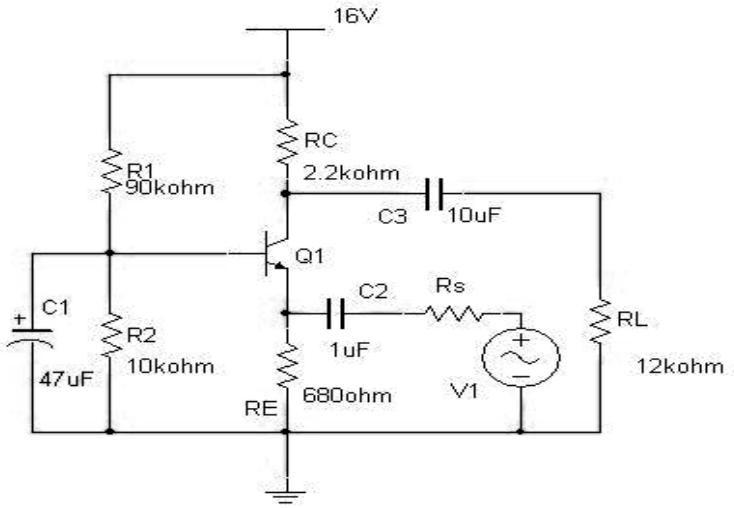
1.a) For the CB amplifier circuit shown, compute R_{IN} and R_{OUT} if C_1 is
i) Connected ii) Not connected
The h-parameters of the transistor in CE configuration are listed as:
h_{ie} = 2.1KΩ, h_{fe} = 81, h_{oe} = 1.66 µMhos and h_{re} is negligibly small.



b) Reason out the causes and results of Phase & Frequency distortions in transistor amplifiers. [9+6]

2.a) Differentiate between direct and capacitive coupling of multiple stages of amplifiers.
b) With the help of a neat circuit diagram, describe the working of a cascode amplifier.
c) What are the merits and demerits of a cascade amplifier over a simple Common Emitter amplifier? [4+7+4]

3.a) Derive the expressions for hybrid Π conductance, $g_{ce,}$ and $g_{bb'}$ of a transistor.
b) Explain how hybrid Π parameters, g_m and g_{ce} vary with I_c, V_{ce} and temperature.
c) Compute the overall lower cut-off frequency of an identical two stage cascade of amplifiers with individual lower cut-off frequency given as 432 Hz. [7+4+4]

4.a) Discuss the effect of different type of loads to a common source MOS amplifier.
b) Differentiate between cascode and folded cascode configurations. [8+7]

5.a) If negative feedback with a feedback factor, β of 0.01 is introduced into an amplifier with a gain of 200 and bandwidth of 6 MHz, obtain the resulting bandwidth of the feedback amplifier.
b) With the help of a suitable BJT based voltage series feedback amplifier diagram, explain the features and benefits of negative feedback in amplifiers. [6+9]

6.a) Substantiate the requirement of positive feedback in amplifier for oscillations. Relate the requirement to Barkhausen Criterion.

b) With the help of neat circuit diagram, explain how sustained oscillations are obtained in RC phase shift BJT based oscillator. Derive the expression for frequency of oscillation. [6+9]

7.a) A single stage class A amplifier V_{cc}=20V, V_{CEQ} =10V, I_{CQ} =600mA, R_L=16 Ω. The ac output current varies by ± 300mA, with the ac input signal. Find

i) The power supplied by the dc source to the amplifier circuit.
ii) AC power consumed by the load resistor.
iii) AC power developed across the load resistor.
iv) DC power wasted in transistor collector.
v) Overall efficiency
vi) Collector efficiency.

b). List the advantages of complementary-symmetry configuration over push pull configuration. [9+6]

8. Describe the following briefly:

a) Stagger Tuned Amplifiers – Operation and comparison with synchronous tuning
b) Heat Sinks for tuned power amplifiers. [8+7]

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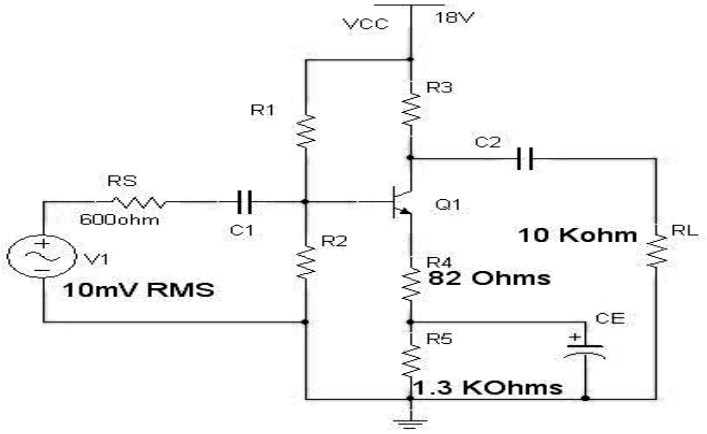
CODE NO: R09220402 | R09 | SET No - 2

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011
ELECTRONIC CIRCUIT ANALYSIS
(Common to Electronics & Communication Systems, Electronics & Computer Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics, Instrumentation & Control Engineering)

Time: 3hours **Max. Marks: 75**

Answer any FIVE questions
All Questions Carry Equal Marks
- - -

1. For the amplifier circuit shown with partially unbypassed emitter resistance, calculate the voltage gain with R_4 in place and with R_4 shorted. Consider h_{ie} = 1.1KΩ, h_{fe} = 100, h_{re} & h_{oe} are negligibly small. Assume R_1 and R_2 to be 100KΩ and 22 KΩ respectively.



b) Analyse what the output voltage should be if the DC power supply given to a CE amplifier is shorted to ground. [10+5]

2.a) With the help of circuit diagram and equivalent circuit of a Darlington amplifier generate the expression for the overall input impedance of the pair.

b) Develop a generalized expression for overall current gain(A_{IS}) when two transistor stages with $R_{OUT2} < R_L$, $R_{OUT1} > R_{IN2}$, $R_{IN1} > R_S$ and individual voltage gains are A_{V1}, A_{V2}. [7+8]

3.a) A transistor amplifier in CE configuration is operated at high frequency with the following specifications. f_T=6MHz, g_m=0.04,h_{fe} =50, $r_{bb'}$ =100 Ω, R_s =500 Ω , $C_{b'c}$ =10pF, R_L=100 Ω. Compute the voltage gain, upper 3dB cut-off frequency, and gain bandwidth product (GBW).

b) Derive an expression for the overall higher cut-off frequency of a two stage amplifier with identical stages of individual higher cut-off frequency, f_H. [7+8]

4.a) Discuss the effect of different type of loads to a common source MOS amplifier.

b) Differentiate between cascode and folded cascode configurations. [8+7]

5.a). If the non-linear distortion in a negative feedback amplifier with an open loop gain of 100 is reduced from 40% to 10%with feedback, compute the feedback factor, β of the amplifier.

b) Draw the circuit diagram of a current series feedback amplifier, Derive expressions to show the effect of negative feedback on input & output impedances, bandwidth, distortion of the amplifier. [6+9]

6.a) Differentiate between RC and LC type oscillators.

b) Derive the expression for frequency of oscillation in a Hartley Oscillator.

c) State Barkhausen Critterion for Oscillations [5+7+3]

7.a) Derive the expression for maximum conversion efficiency for a simple series fed Class A power amplifier.

b) What are the drawbacks of transformer coupled power amplifiers?

c) A push pull amplifier utilizes a transformer whose primary has a total of 160 turns and whose secondary has 40 turns. It must be capable of delivering 40W to an 8 Ω load under maximum power conditions. What is the minimum possible value of V_{cc}? [5+4+6]

8.a) List possible configurations of tuned amplifiers.

b) Derive an expression for bandwidth of a capacitive coupled tuned amplifier in CE configuration. Make necessary assumptions and mention them. [6+9]

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CODE NO: R09220402 | **R09** | **SET No - 3**

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011
ELECTRONIC CIRCUIT ANALYSIS
(Common to Electronics & Communication Systems, Electronics & Computer Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics, Instrumentation & Control Engineering)

Time: 3hours **Max. Marks: 75**

Answer any FIVE questions
All Questions Carry Equal Marks

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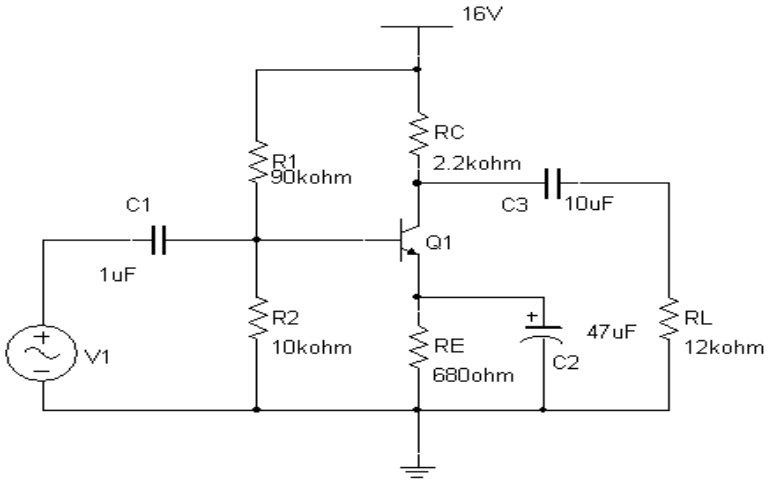
1.a) For the common emitter amplifier shown, draw the AC and DC load lines. Determine the peak-to-peak output voltage for a sinusoidal input voltage of 30mV peak-to-peak. Assume C_1, C_2 and C_3 are large enough to act as short circuit at the input frequency. Consider h_{ie} = 1.1KΩ, h_{fe} = 100, h_{re} & h_{oe} are negligibly small.



b) State Miller's theorem. Specify its relevance in the analysis of a BJT amplifier.
c) Write expressions for A_V and R_{IN} of a Common Emitter amplifier. [7+4+4]

2.a) Derive expressions for overall voltage gain and overall current gain of a two-stage RC coupled amplifier.
b) List out the special features of Darlington pair and cascode amplifiers. [9+6]

3.a) Discuss the effect of emitter bypass capacitor and input & output coupling capacitors on the lower cut-off frequency if number of amplifiers are cascaded.
b) Describe how an emitter follower behaves at high frequencies. [8+7]

4.a) Discuss the effect of different types of loads to a common source MOS amplifier.
b) Differentiate between cascode and folded cascode configurations. [8+7]

5.a) The β and the open loop gain of an amplifier are -10% and -80 respectively. By how much % the closed loop gain changes if the open loop gain increases by 25%?
b) Compare the characteristics of feedback amplifiers in all the four configurations.
c) Reason out why 2 stages are required to implement current shunt feedback. [5+6+4]

6. Starting from the description of a generalized oscillator, derive the expression for frequency of oscillation in a colpitts oscillator. [15]

7.a) With the help of a suitable circuit diagram, show that the maximum conversion efficiency of a class B power amplifier is 78.5%.

b) Explain how Total harmonic distortion can be reduced in a Class B push-pull configured amplifier. [7+8]

8.a) Derive an expression for the bandwidth of a synchronous tuned circuit.

b) Discuss the necessity of stabilization circuits in tuned amplifiers. [8+7]

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CODE NO: R09220402 | R09 | SET No - 4

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011
ELECTRONIC CIRCUIT ANALYSIS
(Common to Electronics & Communication Systems, Electronics & Computer Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics, Instrumentation & Control Engineering)

Time: 3hours **Max. Marks: 75**

Answer any FIVE questions
All Questions Carry Equal Marks

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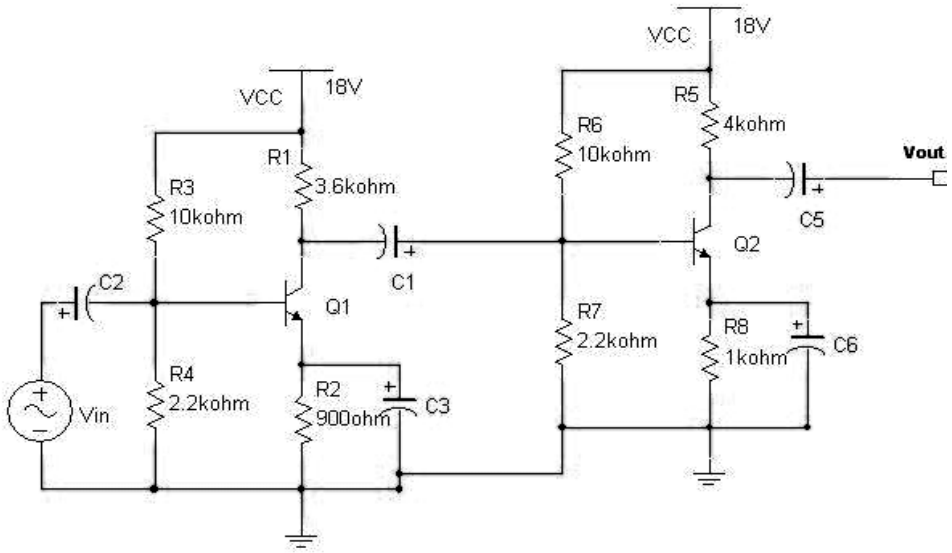
1.a) Draw the circuit diagram of a common collector amplifier along with its equivalent circuit. Derive expressions for A_V and R_I.
b) What is meant by small signal for analyzing a BJT based amplifier?
c) What is non-linear distortion? List the causes for this type of distortion in amplifiers. [7+4+4]

2.a) Discuss various possibilities of inter-stage coupling of amplifiers.
b) For the two-stage RC coupled amplifier circuit shown, calculate the Individual stage voltage gains and the overall voltage gain. Input impedance of individual stages is given as 2.4 KΩ and β of individual transistors as 80. [6+9]



3.a) A transistor has f_α = 8MHz, and β=80.when connected as an amplifier, it has stray capacitance of 100pF at the output terminal. Calculate its upper 3dB frequency when R_{load} is
i) 10KΩ ii) 100KΩ.
b) Discuss the effect of coupling capacitors of a CE amplifier on the overall frequency response of the amplifier. [8+7]

4.a) Discuss the effect of different type of loads to a common source MOS amplifier.
b) Differentiate between cascode and folded cascode configurations. [8+7]

5.a) An amplifier has a gain of 50 with negative feedback. For a specified output voltage, if the input required is 0.1V without feedback and 0.8V with feedback, Compute β and open loop gain.

b) Through the block schematics, show four types of negative feedback in amplifiers.

c) List the advantages of negative feedback in amplifiers. [5+5+5]

6.a) List out the merits × demerits of oscillators.

b) With the help of suitable schematic and description, show that both positive and negative feedback are used in a Wien Bridge oscillator. Establish the condition for oscillations. [7+8]

7.a) State the merits of using push pull configuration? Describe the operation of class B push pull amplifier and show how even harmonics are eliminated.

b) A single ended class A amplifier has a transformer coupled load of 8 Ω. If the transformer turns ration is 10, find the maximum power output delivered to the load. Take the zero signal collector current of 500mA. [7+8]

8.a) Derive the expressions for Bandwidth and Q-factor of single tuned, capacitively coupled amplifiers. List the assumptions made for the derivation.

b) What is stagger tuning? Suggest possible applications. [9+6]

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