Code.No: 33051 | R05 | SET-1

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
II.B.TECH - I SEMESTER SUPPLEMENTARY EXAMINATIONS NOVEMBER, 2009
PULSE AND DIGITAL CIRCUITS
(Common to EEE, ECE, EIE, ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

- - -

1.a) A symmetrical square wave of 10V peak to peak is applied to RC low pass circuit. Draw the output waveforms and find its tilt.
b) Draw the Ringing circuit and explain its operation. [8+8]

2.a) For the circuit shown in fig.1, a sinusoidal voltage of peak 75V is applied. Assume ideal diodes. Obtain the output waveforms.

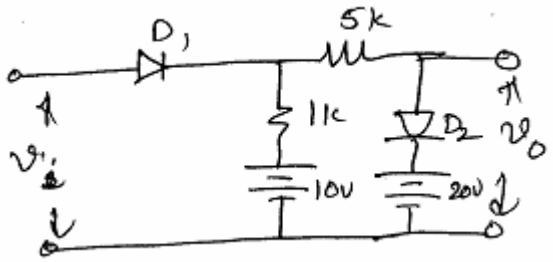

Fig.1

b) Draw the circuit diagram of positive peak clamper circuit. And explain its operation with suitable wave forms. [8+8]

3.a) Explain different switching times of a diode.
b) Explain how saturation parameters are varied with temperature. [8+8]

4.a) Explain different triggering methods of binary circuits.
b) Draw the Schmitt trigger circuit and explain its working. [8+8]

5.a) Explain the following terms.
i) Slope speed error. ii) Displacement error. iii) Transmission error.
b) Explain the working of a transistor current time base generator with the help of a neat circuit. [8+8]

6.a) What is phase jitter? How to avoid it?
b) Explain the frequency division by an Astable blocking oscillator. [8+8]

7.a) Explain the basic principle of sampling gates.
b) What is pedestal? How do we reduce it? [8+8]

8.a) Explain the operation of OR gate using diodes and explain its working with truth table.
b) Compare TTL and RTL logic. [8+8]

Code.No: 33051 | R05 | SET-2

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
II.B.TECH - I SEMESTER SUPPLEMENTARY EXAMINATIONS NOVEMBER, 2009
PULSE AND DIGITAL CIRCUITS
(Common to EEE, ECE, EIE, ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1.a) A ramp input is applied to low pass RC circuit. Draw the response of it and explain its operation.
b) Why attenuator is used in CRO probe. [8+8]

2.a) Draw the emitter coupled clipper circuit and its transfer characteristics and explain its operation.
b) Draw the response of the positive clamping circuit when a square wave input is applied under steady state conditions and explain its operation. [8+8]

3.a) Draw the switching characteristics of Diode and explain it.
b) Define the Breakdown voltages of transistors and explain their significance. [8+8]

4.a) Explain the working of a Bistable multivibrator circuit with the help of waveforms and circuit diagram.
b) Explain how Schmitt trigger circuit act as a switch. [8+8]

5.a) Explain the restoration time and flyback time of time base voltage.
b) With the help of a neat circuit diagram and waveforms explain the working of a transistor miller time base generator. [8+8]

6.a) Compare sine wave synchronization with pulse synchronization.
b) Explain how an Astable multivibrator is used as frequency divider. [8+8]

7.a) Differentiate between unidirectional and bidirectional gates.
b) Draw the sine-diode sampling gate and explain its operation. [8+8]

8.a) Draw the AND gate using diodes and resistors and explain its operation.
b) Draw the Transistor logic NAND gate and explain its operation. [8+8]

Code.No: 33051 | R05 | SET-3

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
II.B.TECH - I SEMESTER SUPPLEMENTARY EXAMINATIONS NOVEMBER, 2009
PULSE AND DIGITAL CIRCUITS
(Common to EEE, ECE, EIE, ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1.a) A symmetrical square wave of ±5V and frequency of 1 kHz applied to a high pass RC circuit having R = 10kΩ and c = 0.05μf. Draw the corresponding output waveform and find its percentage tilt.
b) A rectangular pulse is applied to a RL circuit, draw its response and explain its operation. [8+8]

2.a) Classify different types of clipper circuits. Explain their operation with circuit diagram and its transfer characteristics.
b) What is DC Restorer circuit? Explain its operation. [8+8]

3.a) Draw the piecewise linear characteristics of a transistor and explain its operation.
b) Explain how a transistor works as a switch. [8+8]

4.a) Why commutating capacitor are used in bistable multivibrator?
b) Design a collector coupled monostable multivibrator to be operated from a +50V power supply. The transistor currents are to be 2μA. Assume h_{fe}=50, V_{CE}=0V, V_{BE}=0.7V. [8+8]

5.a) Derive a relation between the slope, transmission and transmission errors.
b) With the help of a neat circuit diagram and waveforms explain the working of a transistor Bootstrap time base generator. [8+8]

6.a) Explain a process of frequency division with sweep circuit.
b) Explain the operation of a monostable multivibrator used as frequency divider. [8+8]

7.a) What are the applications of sampling gates?
b) Draw the four diode sampling gate and explain its operation. [8+8]

8.a) Draw the OR gate using diodes and resistors and explain its working.
b) Draw the NOR gate circuit using transistor and explain its working with truth table. [8+8]

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Code.No: 33051 | R05 | SET-4

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
II.B.TECH - I SEMESTER SUPPLEMENTARY EXAMINATIONS NOVEMBER, 2009
PULSE AND DIGITAL CIRCUITS
(Common to EEE, ECE, EIE, ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

- - -

1.a) Explain how High pass RC circuit work as differentiator.
b) Draw the RC double differentiator circuit and explain its working.
c) Explain the function of RLC ringing circuit. [16]

2.a) The input voltage V_i shown in fig 1(a) is applied to two level clipper shown in fig 1(b). Obtain the output V_o to same scale as V_i. Assume diodes as ideal.

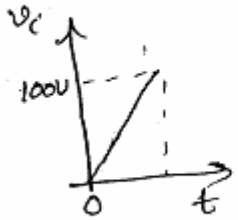

Fig1 (a)

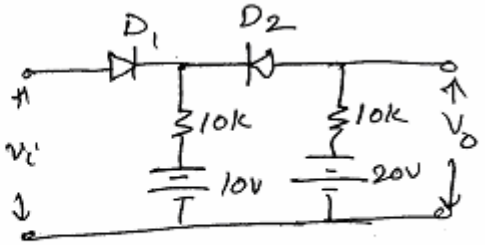

Fig. 1(b)

b) State and prove clamping circuit theorem. [8+8]

3.a) Explain how a diode acts as switch.
b) Explain the saturation parameters of Transistor. [8+8]

4.a) Draw the circuit diagram of Astable multivibrator and explain its working.
b) Distinguish between symmetrical and unsymmetrical triggering methods with relevant circuit diagram. [8+8]

5.a) Explain the basic principles of Miller and Bootstrap time base generator.
b) Explain how linearity is obtained by adjusting the driving waveform of current sweep circuit. [8+8]

6.a) Why synchronization is needed in digital systems?
b) Draw and explain the block diagram of frequency divider. [8+8]

7.a) Differentiate the sampling gates with linear gates.
b) Draw the transistor sampling gate and explain the operation. [8+8]

8.a) Explain the working of INVERTER using transistor and resistors.
b) Compare the Transistor Diode and Resistor Transistor logic. [8+8]

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Code No: 07A4EC07 **R07** **Set No. 2**

II B.Tech II Semester Examinations,APRIL 2011
PULSE AND DIGITAL CIRCUITS
Common to BME, ICE, E.COMP.E, ETM, E.CONT.E, ECE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Explain how a transistor can be used as a switch.
   (b) Explain the phenomenon of 'Latching" in a transistor switch [8+8]

2. (a) Describe the operation of a transistor voltage sweep waveform generator, employing a constant current charging method with the help of its circuit diagram and waveforms.
   (b) Mention the drawbacks of the transistor voltage sweep waveform generator and suggest the methods for eliminating those drawbacks.
   (c) Define sweep speed, Displacement & transmission errors. [6+6+4]

3. (a) Design an astable multivibrator to generate a 5kHz square wave with a duty cycle of 60% and amplitude 12v. Use NPN silicon transistors having $h_{FE(min)}$ = 70, $V_{CE(sat)}$ = 0.3v, $V_{BE(sat)}$ = 0.7v, $V_{BE(cut-off)}$ = 0v and R_C = 2K. Draw the waveforms seen at both collectors and bases.
   (b) Explain the operation of bistable multivibrator circuit with circuit diagram and waveform. [8+8]

4. (a) What is phase delay and phase jitter?
   (b) Explain the method of synchronization of a sinusoidal oscillator with pulses.
   (c) Explain the frequency division in sweep circuit. [4+8+4]

5. (a) Draw the circuit diagram of diode - resistor logic AND gate and explain its operation.
   (b) Design a transistor inverter circuit (NOT gate) with the following specifications. V_{CC} = V_{BB} = 10V, i_{csat} = 10mA; h_{femin} = 30; the input is varying between 0 and 10V. Assume typical junction voltages of npn silicon transistor. [16]

6. (a) What are the applications of sampling gates?
   (b) What are the advantages and disadvantages of unidirectional diode gate?
   (c) Discuss the operation of the four diode bi-directional sampling gate. [4+4+8]

7. (a) A symmetrical square wave of peak -to-peak amplitude 'V' and fequency 'f' is applied to a high pass circuit. Show that the percentage tilt is given by $P = \frac{1-e^{-1/2Rcf}}{1+e^{-1/2Rcf}} \times 100\%$.
   (b) Compare linear waveshaping with NonLinear wave shaping. [8+8]

8. (a) For the clipper circuit shown in figure 1 the input $v_i = 60 \sin \omega t$. Calculate and plot to Scale
   i. The transfer characteristic indicating slopes and intercepts.
   ii. Input / output on the same scale. Assume ideal diodes.

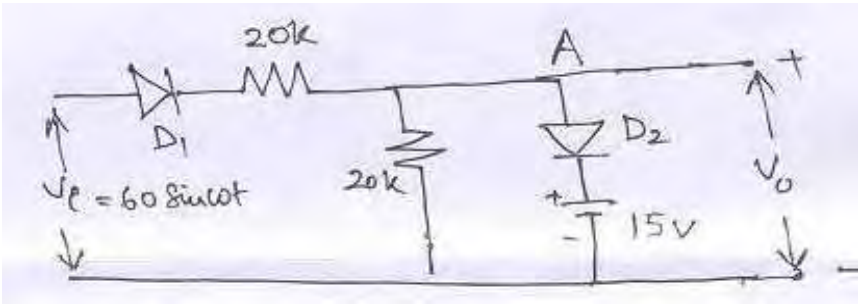

Figure 1:

   (b) Explain positive peak clipping without reference voltage. [12+4]

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Code No: 07A4EC07 **R07** **Set No. 4**

II B.Tech II Semester Examinations,APRIL 2011
PULSE AND DIGITAL CIRCUITS
Common to BME, ICE, E.COMP.E, ETM, E.CONT.E, ECE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) A symmetrical square wave of peak -to-peak amplitude 'V' and fequency 'f' is applied to a high pass circuit. Show that the percentage tilt is given by $P = \frac{1-e^{-1/2Rcf}}{1+e^{-1/2Rcf}} \times 100\%$.
   (b) Compare linear waveshaping with NonLinear wave shaping. [8+8]

2. (a) What is phase delay and phase jitter?
   (b) Explain the method of synchronization of a sinusoidal oscillator with pulses.
   (c) Explain the frequency division in sweep circuit. [4+8+4]

3. (a) Describe the operation of a transistor voltage sweep waveform generator, employing a constant current charging method with the help of its circuit diagram and waveforms.
   (b) Mention the drawbacks of the transistor voltage sweep waveform generator and suggest the methods for eliminating those drawbacks.
   (c) Define sweep speed, Displacement & transmission errors. [6+6+4]

4. (a) Explain how a transistor can be used as a switch.
   (b) Explain the phenomenon of 'Latching" in a transistor switch [8+8]

5. (a) Draw the circuit diagram of diode - resistor logic AND gate and explain its operation.
   (b) Design a transistor inverter circuit (NOT gate) with the following specifications. $V_{CC} = V_{BB} = 10V$, $i_{csat} = 10mA$; $h_{femin} = 30$; the input is varying between 0 and 10V. Assume typical junction voltages of npn silicon transistor. [16]

6. (a) What are the applications of sampling gates?
   (b) What are the advantages and disadvantages of unidirectional diode gate?
   (c) Discuss the operation of the four diode bi-directional sampling gate. [4+4+8]

7. (a) For the clipper circuit shown in figure 2 the input $v_i = 60 \sin \omega t$. Calculate and plot to Scale
      i. The transfer characteristic indicating slopes and intercepts.
      ii. Input / output on the same scale. Assume ideal diodes.
   (b) Explain positive peak clipping without reference voltage. [12+4]

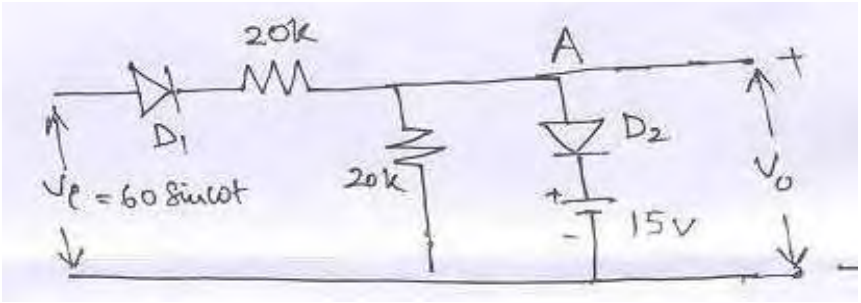

Figure 2:

8. (a) Design an astable multivibrator to generate a 5kHz square wave with a duty cycle of 60% and amplitude 12v. Use NPN silicon transistors having $h_{FE(min)}$ = 70, $V_{CE(sat)}$ = 0.3v, $V_{BE(sat)}$ = 0.7v, $V_{BE(cut-off)}$ = 0v and R_C = 2K. Draw the waveforms seen at both collectors and bases.

   (b) Explain the operation of bistable multivibrator circuit with circuit diagram and waveform. [8+8]

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Code No: 07A4EC07 **R07** **Set No. 1**

II B.Tech II Semester Examinations,APRIL 2011
PULSE AND DIGITAL CIRCUITS
Common to BME, ICE, E.COMP.E, ETM, E.CONT.E, ECE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Explain how a transistor can be used as a switch.
   (b) Explain the phenomenon of 'Latching" in a transistor switch [8+8]
2. (a) What are the applications of sampling gates?
   (b) What are the advantages and disadvantages of unidirectional diode gate?
   (c) Discuss the operation of the four diode bi-directional sampling gate. [4+4+8]
3. (a) Describe the operation of a transistor voltage sweep waveform generator, employing a constant current charging method with the help of its circuit diagram and waveforms.
   (b) Mention the drawbacks of the transistor voltage sweep waveform generator and suggest the methods for eliminating those drawbacks.
   (c) Define sweep speed, Displacement & transmission errors. [6+6+4]
4. (a) Design an astable multivibrator to generate a 5kHz square wave with a duty cycle of 60% and amplitude 12v. Use NPN silicon transistors having $h_{FE(min)}$ = 70, $V_{CE(sat)}$ = 0.3v, $V_{BE(sat)}$ = 0.7v, $V_{BE(cut-off)}$ = 0v and R_C = 2K. Draw the waveforms seen at both collectors and bases.
   (b) Explain the operation of bistable multivibrator circuit with circuit diagram and waveform. [8+8]
5. (a) A symmetrical square wave of peak -to-peak amplitude 'V' and fequency 'f' is applied to a high pass circuit. Show that the percentage tilt is given by $P = \frac{1-e^{-1/2Rcf}}{1+e^{-1/2Rcf}} \times 100\%$.
   (b) Compare linear waveshaping with NonLinear wave shaping. [8+8]
6. (a) What is phase delay and phase jitter?
   (b) Explain the method of synchronization of a sinusoidal oscillator with pulses.
   (c) Explain the frequency division in sweep circuit. [4+8+4]
7. (a) Draw the circuit diagram of diode - resistor logic AND gate and explain its operation.
   (b) Design a transistor inverter circuit (NOT gate) with the following specifications. $V_{CC} = V_{BB}$ = 10V, i_{csat} = 10mA; h_{femin} = 30; the input is varying between 0 and 10V. Assume typical junction voltages of npn silicon transistor. [16]

8. (a) For the clipper circuit shown in figure 3 the input $v_i = 60 \sin \omega t$. Calculate and plot to Scale
   i. The transfer characteristic indicating slopes and intercepts.
   ii. Input / output on the same scale. Assume ideal diodes.

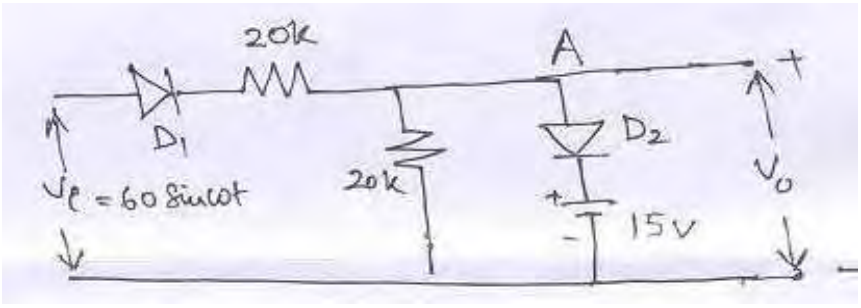

Figure 3:

   (b) Explain positive peak clipping without reference voltage. [12+4]

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Code No: 07A4EC07 **R07** **Set No. 3**

II B.Tech II Semester Examinations,APRIL 2011
PULSE AND DIGITAL CIRCUITS
Common to BME, ICE, E.COMP.E, ETM, E.CONT.E, ECE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw the circuit diagram of diode - resistor logic AND gate and explain its operation.
   (b) Design a transistor inverter circuit (NOT gate) with the following specifications. $V_{CC} = V_{BB} = 10V$, $i_{csat} = 10mA$; $h_{femin} = 30$; the input is varying between 0 and 10V. Assume typical junction voltages of npn silicon transistor. [16]

2. (a) Design an astable multivibrator to generate a 5kHz square wave with a duty cycle of 60% and amplitude 12v. Use NPN silicon transistors having $h_{FE(min)} = 70$, $V_{CE(sat)} = 0.3v$, $V_{BE(sat)} = 0.7v$, $V_{BE(cut-off)} = 0v$ and $R_C = 2K$. Draw the waveforms seen at both collectors and bases.
   (b) Explain the operation of bistable multivibrator circuit with circuit diagram and waveform. [8+8]

3. (a) A symmetrical square wave of peak -to-peak amplitude 'V' and fequency 'f' is applied to a high pass circuit. Show that the percentage tilt is given by $P = \frac{1-e^{-1/2Rcf}}{1+e^{-1/2Rcf}} \times 100\%$.
   (b) Compare linear waveshaping with NonLinear wave shaping. [8+8]

4. (a) What is phase delay and phase jitter?
   (b) Explain the method of synchronization of a sinusoidal oscillator with pulses.
   (c) Explain the frequency division in sweep circuit. [4+8+4]

5. (a) Describe the operation of a transistor voltage sweep waveform generator, employing a constant current charging method with the help of its circuit diagram and waveforms.
   (b) Mention the drawbacks of the transistor voltage sweep waveform generator and suggest the methods for eliminating those drawbacks.
   (c) Define sweep speed, Displacement & transmission errors. [6+6+4]

6. (a) For the clipper circuit shown in figure 4 the input $v_i = 60 \sin \omega t$. Calculate and plot to Scale
      i. The transfer characteristic indicating slopes and intercepts.
      ii. Input / output on the same scale. Assume ideal diodes.
   (b) Explain positive peak clipping without reference voltage. [12+4]

7. (a) Explain how a transistor can be used as a switch.

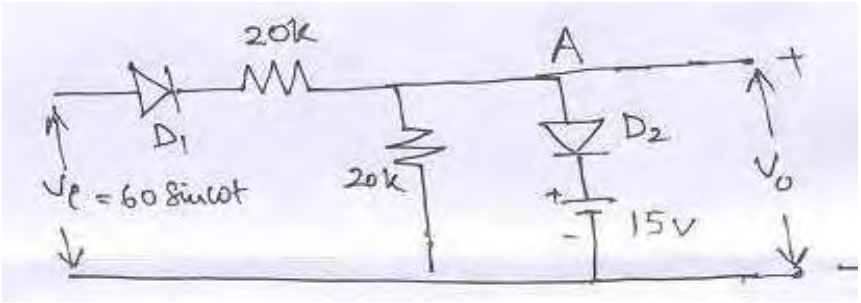

Figure 4:

(b) Explain the phenomenon of 'Latching" in a transistor switch [8+8]

8. (a) What are the applications of sampling gates?
   (b) What are the advantages and disadvantages of unidirectional diode gate?
   (c) Discuss the operation of the four diode bi-directional sampling gate. [4+4+8]

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Code No: 07A30401 **Set No. 1**

II B.Tech I Semester Regular Examinations, November 2008
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the response of RC low pass circuit for exponestial input signal
   (b) Derive the expression for percentage till for a square wave output of Rc high pass circuit. [8+8]

2. (a) Design a diode clamper to restore a d.c level of +3 Volts to an input sinusoidal signal of peak value 10Volts. Assume drop across diode is 0.6 volts as shown in the figure 2a.

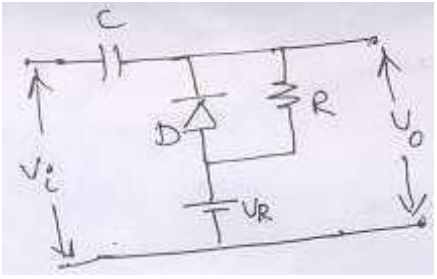

Figure 2a

   (b) Compare series diode clipper and shunt diode clipper. [8+8]

3. (a) Explain the phenomenon of latching in a transistor
   (b) Define the following for a transistor switch
      i. Rise time
      ii. Fall time
      iii. Storage time
      iv. Delay time. [8+8]

4. (a) Explain different triggering methods of binary circuits.
   (b) A collector coupled Fixed bias binary uses NPN transistors with $h_{FE} = 100$. The circuit parameters are V_{CC} = 12v, V_{BB} = -3v, R_C = 1k Ω, R_1 = 5k Ω, and R_2 = 10 k Ω. Verify that when one transistor is cut-off the other is in saturation. Find the stable state currents and voltages for the circuit. Assume for transistors $V_{CE(sat)} = 0.3$V and $V_{BE(sat)} = 0.7$V. [8+8]

5. (a) In a current sweep circuit, explain how linearity correction is made through adjustment of driving waveform.
   (b) Write the basic mechanism of transistor television sweep circuit. [16]

6. (a) What is the condition to be met for pulse synchronization?

(b) Describe synchronization with 2:1 frequency division with neat waveforms.

(c) Define the terms phase delay and phase jitter. [4+8+4]

7. (a) What is a sampling gate.

(b) Illustrate the principle of sampling gates with series and parallel switches and compare them.

(c) Draw the circuit diagram of unidirectional diode gate and explain its operation. [16]

8. (a) Draw the circuit diagram of diode - resistor logic AND gate and explain its operation.

(b) Design a transistor inverter circuit (NOT gate) with the following specifications. $V_{CC} = V_{BB} = 10V$, $i_{csat} = 10mA$; $h_{femin} = 30$; the input is varying between 0 and 10V. Assume typical junction voltages of npn silicon transistor. [16]

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Code No: 07A30401 **Set No. 2**

II B.Tech I Semester Regular Examinations, November 2008
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) A symmetrical square wave whose peak-to-peak amptitude id 2V and whose average value is zero as applied to on Rc integrating circuit. The time constant is equals to half -period of th esquare wave find the peak to peak value of the output amplitude
   (b) Describe the relationship between rise time and RCtime constant of a low pass RC circuit. [8+8]

2. (a) Determine V_o for the network shown in fugure 2a for the given waveform .Assume ideal diodes.

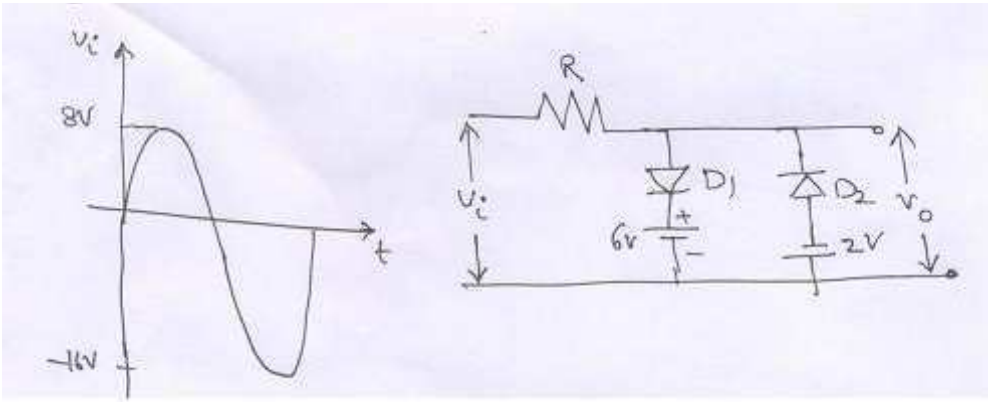

Figure 2a

   (b) Explain negative peak clipper with and without reference voltage. [8+8]

3. (a) For a common emitter circuit $V_{cc} = 10V$, $RC = 1k\Omega$ I_B=0.2A. Determine
      i. The valve of h_{FE}(min) for saturation to occor
      ii. If R_c is changed to 220Ω, will the transistor be saturated
   (b) Explain the phenomenon of latching in a transistor. [8+8]

4. Draw the circuit diagram for Schmitt trigger and explain its operation. What are the applications of the above circuit? Derive the expressions for UTP and LTP. [16]

5. Explain the basic principal of Miller and Bootstrap time base generators and also derive the equations for sweep speed error. [16]

6. (a) With the help of a circuit diagram and waveforms explain frequency division of an a stable multivibrator with pulse signals.

(b) Explain with the help of block diagram and waveforms for acheiving division of relaxation devices without phase jitter. [8+8]

7. (a) Distinguish between sampling gates and logic gates?

   (b) Explain the operation of a chopper amplifier with neat block diagram and waveforms.

   (c) Distinguish between unidirectional and bidirectional gates. [4+8+4]

8. (a) Draw the circuit diagram of diode-transistor logic NOR gate and explain its operation.

   (b) Draw the output waveform X for the given inputs figure 8b

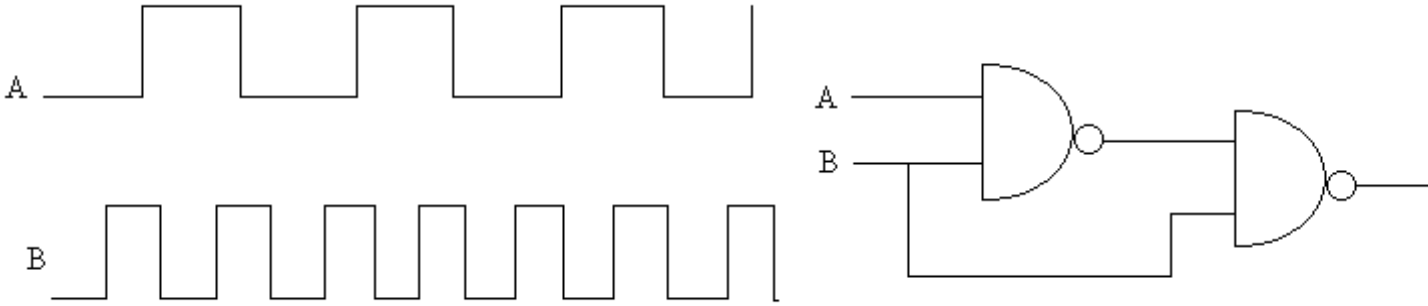

Figure 8b

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Code No: 07A30401 **Set No. 3**

II B.Tech I Semester Regular Examinations, November 2008
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain about RLC Ringing Circuit
   (b) Explain RC double differentiator circuit. [8+8]

2. (a) T=1000 μ sec
   V= 10 V
   Duty cycle = 0.2

   i. Sketch waveform with voltage levels at steady state figure 2(a)iii
   ii. Forward and reverse direction tilt
   iii. A_f / A_r

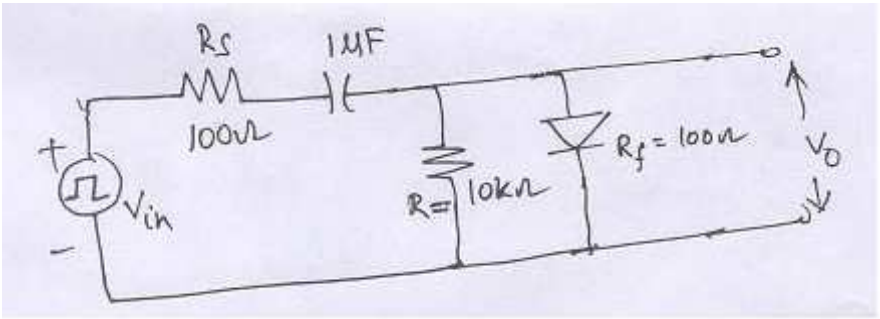

Figure 2(a)iii

   (b) Write a short note on non- linear wave shaping. [12+4]

3. Explain the following
   (a) Storage and transition times of the diode as a switch
   (b) Switching times of the transistor. [8+8]

4. What is a monostable multivibrator? Explain with the help of a neat circuit diagram the principle of operation of a monostable multivibrator, and derive an expression for pulse width. Draw the wave forms at collector and Bases of both transistors. [16]

5. (a) Define sweep time and restoration time of a voltage time base waveform. What is the difference between sweep and sawtooth waveforms?
   (b) In the transistor bootstrap circuit, V_{cc} = 25V, V_{EE} = − 15V, R = 10kΩ, R_E = 15kΩ, R_B = 150 kΩ, C= 0.05 μF, C_1 = 100 μF. The gating waveform has a duration T_G =300 μSec. The transistor parameters are h_{ie} = 1.1 kΩ, h_{re} = 2.5×10^{-4}kΩ, h_{fe} = 50, h_{oe} = 1/40

i. Draw the waveforms of i_c, and v_o, labeling all current and voltage levels.
ii. What is the slope error of the sweep?
iii. What is the sweep speed and the maximum value of the sweep voltage?
iv. What is the retrace time T_r for C to discharge completely?
v. Calculate the recovery time T_1 for C_1 to recharge completely. [16]

6. (a) With the help of a circuit diagram and waveforms, explain frequency division of an astable multivibrator with pulse signals.
   (b) The relaxation oscillator, when running freely, generates an output signal of peak - to - peak amplitude 100V and frequency 1 kHz. Synchronizing pulses are applied of such amplitude that at each pulse the breakdown voltage is lowered by 20V. Over what frequency range may the sync pulse frequency be varied if 1 : 1 synchronization is to result? If 5 : 1 synchronization is to be obtained ($f_P/f_S = 5$), over what range of frequency may the pulse source be varied? [16]

7. (a) Explain the operation of a six - diode gate.
   (b) Write the applications of sampling gates.
   (c) Briefly describe the chopper amplifier and sampling scope. [16]

8. (a) Compare the Resistor Transistor logic and Diode Transistor logic families
   (b) Explain the wired AND logic with the help of circuit diagram. [8+8]

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Code No: 07A30401 **Set No. 4**

II B.Tech I Semester Regular Examinations, November 2008
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Obtain the response of RC high pass cirucit for an exponential i/p lignal
   (b) A square wave whose peak-to-peak valve is IV, exterds I 0.5V w.r.t. to ground. The half period is O.iSec this voltage impressed upon an RC differentating circuit whose time constant is 0.2 sec. Determine the maximum and minimum valves of the l/p voltages int eh steady state. [8+8]

2. (a) The input voltage v_i to the two level clipper shown in figure 2a varies linearly from 0 to 75 V. Sketch the output voltage v_o to the same time scale as the input voltage. Assume Ideal diodes.

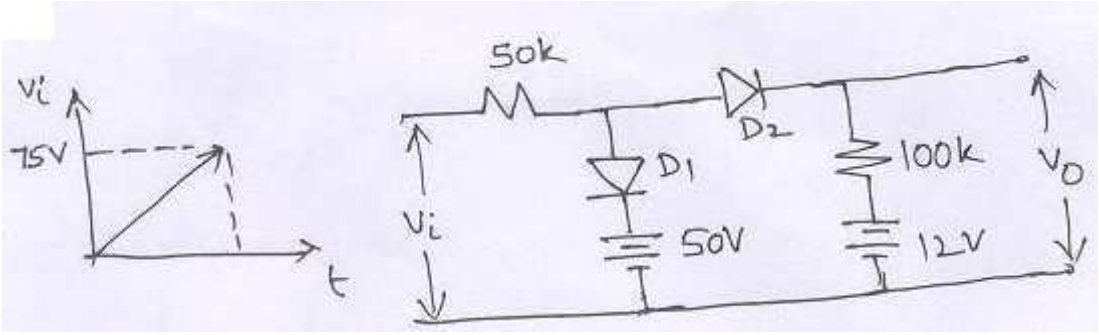

Figure 2a

   (b) Explain positive peak voltage limiters below reference level. [12+4]

3. (a) Explain with relevant diagram the various transistor switching times
   (b) Explain the storage and transition times of the diode as a switch. [8+8]

4. Explain about various switching conditions of Schmitt trigger. [16]

5. (a) What are the methods of generating a time base waveform? Explain each method.
   (b) Derive the expression Mathematical relationship between sweep speed error, Displacement error and transmission error for an exponential sweep circuit. [16]

6. (a) Describe frequency division employing a transistor a stable multivibrator with waveforms.
   (b) Describe frequency division employing a transistor monostable multivibrator with waveforms. [8+8]

7. (a) Describe the working of a four diode gate with necessary diagrams and equations.

   (b) For the four diode gate, $R_L = R_C = 100k\ \Omega$ and that $R_2 = 2k\Omega$, $R_F = 50\Omega$. For $V_s = 25V$, compute gain A, V_{min} and $(V_c)_{min}$. Compute $(V_n)_{min}$ for V $= V_{min}$.

   [16]

8. (a) Define positive and negative logic system

   (b) Define fan-In, fan-out

   (c) Draw and explain the circuit diagram of a diode OR gate for positive logic.

   [4+4+8]

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