Code No: 09A31002 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year I Semester Examinations, June/July-2014
SWITCHING THEORY AND LOGIC DESIGN
(Common to EIE, ECOMPE)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Convert the following hexadecimal numbers to their decimal equivalents:
i) 888.8
ii) EBA.C.

b) Perform the following subtraction using 1's complement:
i) 5-7
ii) 7- 5.

c) Explain error detection using Hamming code with an example.

2.a) Show that the dual of exclusive OR is equal to its complement.

b) Reduce the following Boolean expression to one literal
$$A'B(D'+C'D)+B(A+A'CD)$$

c) Implement the following Boolean expression using minimum number of NAND gates only.
$$\overline{A}\,.\,\overline{B}+A\,.\,\overline{B}=Y$$

3.a) Use a k-map to simplify the following Boolean expression
$$y=\overline{C}(\overline{A}\,\overline{B}\,\overline{D}+D)+A\overline{B}C+\overline{D}$$

b) Simplify the Boolean function using tabular method
$$F(A,B,C,D)=\sum(1,2,3,9,12,13,14)+\sum_{\phi}(0,7,10,15)$$

4.a) Implement the following function using a 8:1 multiplexer
$$F(A,B,C,D)=\sum(0,1,3,4,8,9,15)$$

b) Implement a 3 bit binary to gray code converter using logic gates.

5.a) Implement a BCD to Excess-3 converter using PLA.

b) Implement the following functions using a PAL.
$$F_1(A,B,C,D)=\Sigma(0,1,5,6,11)$$
$$F_2(A,B,C,D)=\Sigma(0,2,7,9,13)$$

6.a) Implement a modulo 6 ring counter and explain using relevant truth table and also draw its state diagram assuming a necessary initial state.

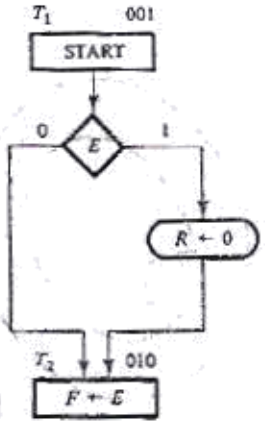
b) Explain the functionality of a J-K flip-flop using truth table. Also obtain its excitation table.

7.a) Compare and contrast Melay and Moore machines.

b) Simplify the sequential machine represented by the state table shown below using Merger graph.

	NS, z			
PS	I_1	I_2	I_3	I_4
A	—	C, 1	E, 1	B, 1
B	E, 0	—	—	—
C	F, 0	F, 1	—	—
D	—	—	B, 1	—
E	—	F, 0	A, 0	D, 1
F	C, 0	—	B, 0	C, 1

8.a) Explain how ASM chart is different from a conventional flow chart? Using the figure shown below show the difference in interpretation.



b) Draw the ASM chart for a binary multiplier.

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year I Semester Examinations, November/December - 2013
SWITCHING THEORY AND LOGIC DESIGN

Time: 3 hours **Max. Marks: 75**

Answer any five questions

All questions carry equal marks

1. a) Perform the following using BCD arithmetic. [4M]
   i) 812410 + 812710
   b) Convert the following. [8M]
   (i) $AB_{16} = (\ )_{10}$ (ii) $1234_8 = (\ )_{10}$ iii) $(10110011)_2 = (\ )_{10}$ (iv) $772_{10} = (\ )_{16}$

2. a) State and prove the following Boolean laws. [4M]
   (i) Associative (ii) Distributive
   b) Find the complement of the following Boolean functions and reduce them to minimum Number of literals: (i) (bc'+ a'd) (ab' + cd') (ii) b'd + a'bc' + acd + a'bc [8M]

3. a) What are the advantages of Tabulation method over K-map? [2M]
   b) Simplify the following Boolean function using Tabulation method. [10M]
   $Y(A,B,C,D) = \sum(1,3,5,8,9,11,15)$

4. a) Express the Boolean function F=A + B'C in canonical SOP form. [6M]
   b) Express the Boolean function F= xy + x'z in canonical POS form. [6M]

5. a) Design a combinational circuit with three inputs and one output. [6M]
   The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise
   b) Design 3 bit binary to gray code converter. [6M]

6. a) Explain operation of JK flip-flop with the help of circuit diagram. [6M]
   b) Design 3bit synchronous down counter using T flip-flops. [6M]

7. a) Write the differences between Mealy and Moore type machines. [6M]
   b) List out capabilities and limitations of finite state machines [6M]

8. a) Explain the operation of ring counter. What are its applications? [6M]
   b) Design a counter with the following repeated binary sequence 0,1,2,4,6 using D flip-flops. [6M]

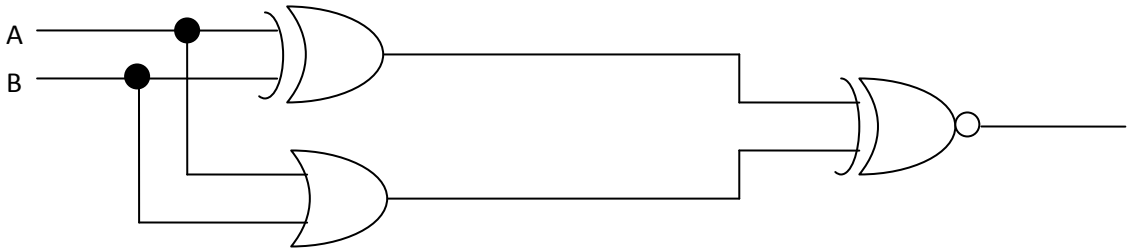
JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year I Semester Examinations, May/June - 2014
SWITCHING THEORY AND LOGIC DESIGN

Time: 3 hours **Max. Marks: 75**

Answer any five questions

All questions carry equal marks

1. a) Determine the canonical POS form for the function f(x,y,z)=x(y^1+z) [6M]
   b) Redraw the given circuit in fig shown below after simplification. (Diagram) [6M]



2. a) What is gray code? What are the rules to construct the gray code? Develop the 4-bit gray code for the decimal 0 to 15. [6M]
   b) (i) Why the Binary number system is used in Computer Design. [3M]
   (ii) What are the universal gates? Why so it is called universal gates. Justify with one or two examples. [3M]

3. a) What do you mean by K-map? Name its Advantages and Disadvantages. [6M]
   b) Reduce the following using K-map and implement it using NAND logic F = $\sum m(0,2,3,4,5,6)$. [6M]

4. a) Design a BCD to excess-3 code converter. [6M]
   b) Design 4-bit even parity generator. Mention Truth Table. [6M]

5. a) Implement the following Boolean function using 8:1 mux consider 'A' as the I/P and BCD as selection lines. F(A,B,C,D)= A $\overline{B}$ +BD+ $\overline{B}$ C $\overline{D}$. [4M]
   b) Implement the following function using Decoder.
   (i) F (W,X,Y,Z) = $\sum$ (1, 9, 12, 15)
   (ii) H (W, X, Y, Z) = $\sum m$ (0, 1, 2, 3, 4, 5, 7, 8, 11, 12, 14) [8M]

6. a) Design a sequential ckt with two D-Flip Flops 'A' and 'B' and one input x. When x = 0, state of the circuit remaining the same. When x=1 the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00 and repeats. [6M]
   b) What do you mean by triggering? Explain the various triggering modes with examples. [6M]

7. a) Explain the SR- Flip- Flop and JK Flip- Flop with NAND diagrams. [6M]
   b) Design Mod-5 counter to count the sequence 0,1, 3, 7,6. Your design should include circuitry to ensure that if we end up in an unused state, the next clock pulse will reset the counter to $\theta_2\theta_1\theta_0$ =000. Use JK Flip-Flops. [6M]

UNIT – V

8. a) Convert the following mealy machine into a corresponding Moore machine. [6M]

PS	NS, Z	
	X=0	X=1
A	C, 0	B, 0
B	A, 1	D, 0
C	B, 1	A, 1
D	D, 1	C, 0

b) Using shift register, how do you obtain a circular shift? [6M]