INSTITUTE OF AERONAUTICAL ENGINEERING

(AUTONOMOUS)

Code No: **BES005**

MODEL QUESTION PAPER - II

M-Tech I Semester Regular Examinations, February 2017

FPGA ARCHITECTURE AND APPLICATIONS

(Embedded Systems)

Time: 3 hours Max. Marks: 70

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT I

1.	(a)	Explain in detail about CPLD architectures.	[7M]
	(b)	Design a 1 bit magnitude comparator using PROM.	[7M]
2.	(a)	Mention the features of generic array logic over PLDs.	[7M]
	(b)	Describe the functional blocks of XCR3064XL CPLD.	[7M]

UNIT II

3.	(a)	List the different components of FPGA.	[7M]
	(b)	Describe the function of programming interconnects in FPGA.	[7M]
4.	(a)	Discuss the different programming technologies in FPGA.	[7M]
	(b)	Explain in detail about programmable logic blocks in FPGA.	[7M]

UNIT III

5.	(a)	Draw the simplified block diagram for Xilinx XC4000 series CLB.	[7M]
	(b)	With neat diagram, discuss the function of XILINX XC 2000 architecture.	[7M]
6.	(a)	Why SRAM based FPGAs are popular when compared to other types?	[7M]
	(b)	Explain the architecture of XILINX XC 3000 architecture.	[7M]

UNIT IV

7.	(a)	Discuss the features of ACT 3 architecture.	[7M]

(b) Discuss the concept of Shannon expansion theorem in ACT architectures. [7M]

8. (a) Explain the functional blocks of ACT 2 architecture. [7M]

(b) Describe the functionality of ACT 1 architecture. [7M]

UNIT V

9. (a) Design a synchronous counter using ACT devices. [7M]

(b) Discuss the concept of position tracker in robot manipulator. [7M]

10. (a) Mention the design issues of ACT architectures. [7M]

(b) Design a adder using ACT architectures. [7M]