Hall Ticket No | | | | | | | | | | |

Question Paper Code: ACSB07

INSTITUTE OF AERONAUTICALENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

MODEL QUESTION PAPER-I

B.Tech IV Semester End Examinations, April - 2020
Regulation: R18
COMPUTER ORGANIZATION
(Common to CSE/IT)

Time: 3Hours **Max Marks:70**

Answer any ONE question from each Unit All
questions carry equal marks
All parts of the question must be answered in one place only

MODULE – I

1	a)	What is memory address register (MAR) and memory data register (MDR) and Describe the IEEE standard for floating point numbers for single precisionnumber.?	[7M]
	b)	Explain instruction formats for various types of computer organizations as single accumulator, general register andstack?	[7M]
2	a)	Explain the issues to be consider in accumulator based CPU with respect to programming considerations, instruction set.	[7M]
	b)	Illustrate the diagram for connection between the processor and the memory and explain basic operational concepts of computer.	[7M]

MODULE – II

3	a)	Write short notes on the following i. CPU-IOPcommunication ii. Micro programsequencer iii. Floating point arithmetic (addition andmultiplication).	[7M]
	b)	Explain Booth's multiplication algorithm for signed 2's complement numbers in details, with a suitable example and give the hard ware requirement.	[7M]
4	a)	What is pipelining, branch penalty, and Draw the floating point addition subtraction unit neatly and explain the operation?	[7M]
	b)	Derive an algorithm in flow chart form for non-restoring algorithm method of fixed point binary division?	[7M]

MODULE – III

5	a)	Write control signals for storing a word in memory and Draw a block diagram of control signal for register MDR?	[7M]
	b)	Explain in detail the decoding and encoding function of hardwired control unit and Compare hardwired control unit and micro programmed control unit?	[7M]

6 a) Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome/minimize these hazards. [7M]

b) Explain in detail regarding the implementation requirements of the pipeline? [7M]

MODULE – IV

7 a) Write formula for calculating the average access time experienced by the processor in a system with two level of caches? [7M]

b) Explain the following nodes of transfer in brief : [7M]

i. Interrupt – initiatedI/O
ii. DMA.
iii. Explain the methods employed for establishing priority for simultaneous interrupts.

8 a) Draw the organization of the serial access memory unit and explain its accessing mechanism? [7M]

b) Criticize the following statement: "Using the faster processing chip results in a corresponding increase in the performance of computer even if the main memory speed remains the same". [7M]

MODULE – V

9 a) What are the three different mechanism commonly used in bus arbitrationand What are the various mechanism for implementing i/o operation? [7M]

b) Write a short notes on the following: [7M]

i. RISC/CISC –Differentiate.
ii. Stored programorganization

10 a) Write notes on: [7M]

i. Polling
ii. VectoredInterrupts
iii. SynchronousI/O
iv. AsynchronousI/O

b) Write a program to evaluate the arithmetic statement: X = (A - B + C * (D* E - f)) / (G + H*K) [7M]

a. Using a general register computer with three address instructions.
b. Using a general register computer with two addressinstructions.
c. Using an accumulator type computer with one address instructions.
d. Using a stack organized computer with zero-address operationinstructions.

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I. COURSEOBJECTIVES:

The course should enable the students to:

S. No	Description
I	Understand the organization and architecture of computer systems and electronic computers.
II	Study the assembly language program execution, instruction format and instruction cycle.
III	Design a simple computer using hardwired and micro programmed control methods.
IV	Study the basic components of computer systems besides the computer arithmetic
V	Understand input-output organization, memory organization and management, and pipelining.

II. COURSE OUTCOMES:

The course should enable the students to:

CO 1	Understand the organization and levels of design in computer architecture
CO 2	Ability to learn the concepts of instruction set formats
CO 3	To understand the concepts of programming methodologies
CO 4	Ability to learn virtual memory concept with page replacement concept in memory organization
CO 5	Understand the different priority interrupts in the input-output organization in the computer architecture.

III. COURSE LEARNINGOUTCOMES:

At the end of the course, the student will have the ability to:

S. No	CLO's	Description
ACSB07.01	CLO 1	Describe the various components like input/output units, memory unit, control unit, arithmetic logic unit connected in the basic organization of a computer.
ACSB07.02	CLO 2	Understand the interfacing concept with memory subsystem organization and input/output subsystem organization.
ACSB07.03	CLO 3	Understand instruction types, addressing modes and their formats in the assembly language programs.
ACSB07.04	CLO 4	Describe the instruction set architecture design for relatively simple microprocessor or Central Processing Unit.
ACSB07.05	CLO 5	Classify the functionalities of various micro operations such as arithmetic, logic and shift micro operations.
ACSB07.06	CLO 6	Understand the register transfer languages and micro operations involved in bus and memory transfers.
ACSB07.07	CLO 7	Describe the design of control unit with address sequencing and microprogramming Concepts.
ACSB07.08	CLO 8	Understand the connections among the circuits and the functionalities in the hardwired control unit.
ACSB07.09	CLO 9	Describe the various phases involved in the instruction cycle viz. fetching, Decoding, reading effective address and execution of instruction.
ACSB07.10	CLO 10	Describe various data representations and explain how arithmetic and logical operations are performed by computers.
ACSB07.11	CLO 11	Classify the various instructions formats tosolve the arithmetic expressions in different addressing modes.
ACSB07.12	CLO 12	Understand the functionality of various instruction formats for writing assemblylanguage programs.
ACSB07.13	CLO 13	Describe the implementation of fixed pointand floating point addition, subtraction operations.
ACSB07.14	CLO 14	Understand the concept of memory hierarchyand different typed of memory chips.
ACSB07.15	CLO 15	Describe various modes of data transferbetween CPU and I/O devices

ACSB07.16	CLO 16	Understand the virtual memory concept with page replacement concept in memory organization
ACSB07.17	CLO 17	Describe the hardware organization of associate memory and understand the readand write operations
ACSB07.18	CLO 18	Describe the parallel processing concept withmultiple functional units.
ACSB07.19	CLO 19	Understand the multiprocessor concept with system bus structure and the concept of inter processor communication andsynchronization.
ACSB07.20	CLO 20	Understand the different priority interrupts in the input-output organization in the computerarchitecture.
ACSB07.21	CLO 21	Possess the knowledge and skills for employability and to succeed in nationaland International level competitiveexaminations.
ACSB07.22	CLO 22	Possess the knowledge and skills to design advanced computer architecture for currentindustry requirements.

IV. MAPPING OF SEMESTER END EXAMINATION TO COURSE LEARNINGOUTCOMES:

SEE Question No.		Course Learning Outcomes		CO'S	Blooms Taxonomy Level
1	a	ACSB07.01	Describe the various components like input/output units,memory unit, control unit, arithmetic logic unit connected in the basic organization of acomputer.	CO1	Understand
	b	ACSB07.02	Describe the various components like input/output units, memory unit, control unit, arithmetic logic unit connectedin the basic organization of a computer.	CO1	Understand
2	a	ACSB07.03	Understand instruction types, addressing modes and theirformats in the assembly language programs.	CO1	Understand
	b	ACSB07.04	Describe the implementation of fixed point and floatingpoint addition, subtraction operations.	CO1	Understand
3	a	ACSB07.05	Describe the various major algorithmictechniques Robertson algorithm, booth's algorithm, no restoring division algorithm.	CO2	Understand
	b	ACSB07.06	Describe the pipeline processing concept with multiple functional units.	CO2	Understand
4	a	ACSB07.07	Illustrate the connections among the circuits and thefunctionalities in the hardwired control unit.	CO2	Understand
	b	ACSB07.08	Describe the design of control unit with address sequencing and microprogramming Concepts.	CO2	Remember
5	a	ACSB07.09	Understand the functionality of super scalar processing and Nano programming.	CO3	Understand
	b	ACSB07.10	Understand the concept of memory hierarchy and differenttyped of memory chips.	CO3	Remember
6	a	ACSB07.11	Understand the cache and virtual memory concept in memory organization.	CO3	Understand
	b	ACSB07.12	Describe the hardware organization of associate memoryand understand the read and write operations.	CO3	Understand
7	a	ACSB07.13	Understand the various bus control interfaces and system control interfaces.	CO4	Understand
	b	ACSB07.13	Describe the various interrupts like Vectored Interrupts, PCI interrupts, Pipeline interrupts.	CO4	Understand
8	a	ACSB07.14	Understand the functionally of RISC and CISC processor.	CO4	Understand
	b	ACSB07.14	Possess the knowledge and skills for employability and to succeed in national and international level competitiveexaminations.	CO4	Understand
9	a	ACSB07.15	Possess the knowledge and skills to design advancedcomputer architecture for current industry requirements.	CO5	Understand
	b	ACSB07.15	Formulate and analyze the smith chart to estimateimpedance, VSWR, reflection coefficient, OC and SC lines.	CO5	Remember

SEE Question No.		Course Learning Outcomes		CO'S	Blooms Taxonomy Level
10	a	ACSB07.16	Formulate and analyze the smith chart to estimateimpedance, VSWR, reflection coefficient, OC and SC lines.	CO5	Understand
	b	ACSB07.16	Formulate and analyze the smith chart to estimateimpedance, VSWR, reflection coefficient, OC and SC lines.	CO5	Remember

Signature ofCourse Coordinator **HOD, IT.**