INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)
Dundigal, Hyderabad - 500043, Telangana

ELECTRONICS AND COMMUNICATION ENGINEERING
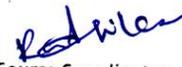## ATTAINMENT OF COURSE OUTCOME - ACTION TAKEN REPORT

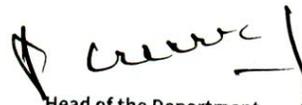|			
Name of the faculty:	**Ms. C RADHIKA**	Department:	**Electronics and Communication Engineering**
Regulation:	**IARE - BT23**	Batch:	**2023-2027**
Course Name:	**Digital System Design Laboratory**	Course Code:	**AECD07**
Semester:	**III**	Target Value:	**60% (1.8)**

Attainment of COs:

	Course Outcome	Direct Attainment	Indirect Attainment	Overall Attainment	Observation
CO1	Utilize the concept of Boolean algebra to verify the truth table of Boolean expressions using logic gates in Hardware Description Language.	1.80	0.00	1.8	Attained
CO2	Make use of dataflow, structural and behavioral modelling styles of HDL for simulating the combinational logic circuits.	1.80	0.00	1.8	Attained
CO3	Analyze the truth tables and characteristic equations of flip flops for the functional simulation and timing analysis of sequential circuits.	1.80	0.00	1.8	Attained
CO4	Construct the synchronous and asynchronous sequential circuits using the flip flops.	1.80	0.00	1.8	Attained
CO5	Model a finite state machine with melay and moore machines for detecting or generating a given sequence.	1.80	0.00	1.8	Attained
CO6	Examine the functionality of Vending machine controller,time traffic light controller, chess clock controller FSM, elevator operations using HDL code.	1.80	0.00	1.8	Attained

Action Taken Report: (To be filled by the concerned faculty / course coordinator)

Course Coordinator   **Mentor**   **Head of the Department**

Dr. P. MUNASWAMY M.Tech, Ph.D, MISTE
Professor & Head
ELECTRONICS AND COMMUNICATION ENGINEERING
INSTITUTE OF AERONAUTICAL ENGINEERING
Dundigal, Hyderabad- 500 043, T.S.