



# INSTITUTE OF AERONAUTICAL ENGINEERING (Autonomous)

Dundigal, Hyderabad - 500043, Telangana

## ELECTRONICS AND COMMUNICATION ENGINEERING

### ATTAINMENT OF COURSE OUTCOME - ACTION TAKEN REPORT

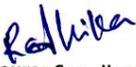
Name of the faculty: **Ms. C RADHIKA** Department: **Electronics and Communication Engineering**  
Regulation: **IARE - BT23** Batch: **2023-2027**  
Course Name: **Digital System Design** Course Code: **AECD03**  
Semester: **III** Target Value: **60% (1.8)**

#### Attainment of COs:

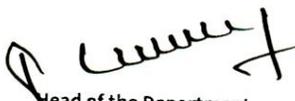
Course Outcome	Direct Attainment	Indirect Attainment	Overall Attainment	Observation
CO1 Outline binary arithmetic operations and optimize boolean functions using karnaugh and tabulation method.	3.00	2.30	2.9	Attained
CO2 Make use of basic logic gates to realize the combinational logic circuits used in conventional electronic circuits	2.60	2.30	2.5	Attained
CO3 Interpret the knowledge of flip-flops and latches in synchronous and asynchronous modules for memory storing applications.	1.80	2.30	1.9	Attained
CO4 Develop Mealy/Moore models and state diagrams for the complex sequential circuit applications.	1.80	2.30	1.9	Attained
CO5 Identify the different logic families, memories and programmable logic devices for understanding the architectural blocks of FPGA	2.40	2.30	2.4	Attained
CO6 Demonstrate the different modelling styles and data types in VHDL for implementing combinational and sequential circuits.	1.20	2.30	1.4	Not Attained

#### Action Taken Report: (To be filled by the concerned faculty / course coordinator)

CO6: Assignments will be given on different modelling styles and data types in VHDL for implementing combinational and sequential circuits.

  
Course Coordinator

  
Mentor

  
Head of the Department

**Dr. P. MUNASWAMY** M.Tech, Ph.D, MISTE  
Professor & Head  
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