INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)

Dundigal, Hyderabad - 500043, Telangana

ELECTRONICS AND COMMUNICATION ENGINEERING

ATTAINMENT OF COURSE OUTCOME - ACTION TAKEN REPORT

Name of the faculty:	Ms. B VEENA	Department:	Electronics and Communication Engineering
Regulation:	IARE - R20	Batch:	2021-2025
Course Name:	Digital System Design	Course Code:	AECC03
Semester:	III	Target Value:	60% (1.8)
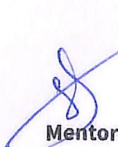
Attainment of COs:
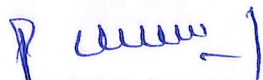
	Course Outcome	Direct Attainment	Indirect Attainment	Overall Attainment	Observation
CO1	Outline binary arithmetic operations and optimize boolean functions using karnaugh and tabulation method.	2.30	2.30	2.3	Attained
CO2	Make use of basic logic gates to realize the combinational logic circuits used in conventional electronic circuits	2.70	2.20	2.6	Attained
CO3	Interpret the knowledge of flip-flops and latches in synchronous and asynchronous modules for memory storing applications.	1.30	2.20	1.5	Not Attained
CO4	Develop Mealy/Moore models and state diagrams for the complex sequential circuit applications.	2.30	2.20	2.3	Attained
CO5	Identify the different logic families, memories and programmable logic devices for understanding the architectural blocks of FPGA	2.30	2.20	2.3	Attained
CO6	Demonstrate the different modelling styles and data types in VHDL for implementing combinational and sequential circuits.	3.00	2.20	2.8	Attained

Action Taken Report: (To be filled by the concerned faculty / course coordinator)

CO3: Guest lectures will be conducted on flip-flops and latches in synchronous and asynchronous modules for memory storing applications

Course Coordinator

Mentor

Head of the Department

Dr. P. MUNASWAMY M.Tech, Ph.D, MISTE
Professor & Head
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