INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)
Dundigal, Hyderabad - 500043, Telangana

ELECTRONICS AND COMMUNICATION ENGINEERING

ATTAINMENT OF COURSE OUTCOME - ACTION TAKEN REPORT

Name of the faculty:	**Ms. Y MEGHAMALA**	Department:	**Electronics and Communication Engineering**
Regulation:	**IARE - R20**	Batch:	**2020-2024**
Course Name:	**Digital design through Verilog**	Course Code:	**AECC49**
Semester:	**VII**	Target Value:	**60% (1.8)**

Attainment of COs:

	Course Outcome	Direct Attainment	Indirect Attainment	Overall Attainment	Observation
CO1	Describe the basic language elements and data flow modelling constructs to implement the combinational and sequential circuits in Verilog	2.70	2.20	2.6	Attained
CO2	Utilize the basic logic gate primitives and user defined primitives for implementing digital circuits in gate level modelling	2.40	2.10	2.3	Attained
CO3	Illustrate the significance of structured procedures in behavioral modeling using blocking and nonblocking procedural assignments	2.30	2.10	2.3	Attained
CO4	Make use of loop and conditional statements to describe the digital circuits in behavioral modeling	3.00	2.10	2.8	Attained
CO5	Identify the methods to specify delays on switch primitives for designing modules with time delays in switch level modeling	3.00	2.10	2.8	Attained
CO6	Distinguish the synchronous and asynchronous sequential state machines for synthesizing the sequential circuits	2.30	2.10	2.3	Attained

Action Taken Report: (To be filled by the concerned faculty / course coordinator)

Course Coordinator

Mentor

Head of the Department

Dr. P. MUNASWAMY M.Tech, Ph.D, MISTE
Professor & Head
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