INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

ATTAINMENT OF COURSE OUTCOME- ACTION TAKEN REPORT

Name of the Faculty:	**Ms. B Veena**	Department:	**ECE**
Regulation:	**R18**	Batch:	**2019-2023**
Course Name:	**Digital design through Verilog**	Course Code:	**AECB44**
Semester:	**VII**	Target Value:	**60% (1.8)**

Attainment of COs:

Course Outcome		Direct Attainment	Indirect Attainment	Overall Attainment	Observations
CO1	Summarize the basic language elements and data flow modelling constructs to implement the combinational and sequential circuits in Verilog.	3	2.1	2.8	Target Attained
CO2	Utilize the basic logic gate primitives and user defined primitives for implementing digital circuits in gate level modelling.	3	2.1	2.8	Target Attained
CO3	Illustrate the significance of structured procedures in behavioral modeling using blocking and nonblocking procedural assignments.	3	2.1	2.8	Target Attained
CO4	Make use of loop and conditional statements to describe the digital circuits in behavioral modeling.	3	2.1	2.8	Target Attained
CO5	Identify the methods to specify delays on switch primitives for designing modules with time delays in switch level modeling.	3	2.1	2.8	Target Attained
CO6	Examine the synchronous and asynchronous sequential state machines for synthesizing the sequential circuits.	3	2.1	2.8	Target Attained

Course Coordinator **Mentor** **HOD**

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