INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

ATTAINMENT OF COURSE OUTCOME- ACTION TAKEN REPORT

Name of the Faculty:	Dr V. Vijay	Department:	ECE
Regulation:	IARE-R16	Branch:	2017-2021
Course Name:	Digital System Design Laboratory	Course Code:	AEC103
Semester:	IV	Target Value:	60% (1.8)

Attainment of COs:

	Course Outcome	Overall Attainment	Observations
CO1	Apply the concept of Boolean algebra to verify the truth table of various expressions using logic gates in Hardware Description Language.	2	Attainment target reached
CO2	Make use of dataflow, structural and behavioural modelling styles of HDL for simulating the combinational logic circuits.	2	Attainment target reached
CO3	Analyze the SR flip flop, JK flip flop, D flip flop, T flip flops for functional simulation and timing analysis.	2	Attainment target reached
CO4	Build the universal shift registers, counters using the flip flops.	2	Attainment target reached
CO5	Examine a finite state machine for detection of sequence.	2	Attainment target reached
CO6	Design the real time applications like traffic light controller, chess clock controller FSM, elevator operations using FPGA kit.	2	Attainment target reached

Course Coordinator

Mentor

HOD

Head of the Department
Electronics and Communication Engineering
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