INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

ATTAINMENT OF COURSE OUTCOME- ACTION TAKEN REPORT

Name of the Faculty:	Mr.K Chaithanya	Department:	ECE
Regulation:	IARE-R16	Batch:	2016-2020
Course Name:	Digital Signal Processors and Architecture	Course Code:	AEC507
Semester:	VIII Semester	Target Value:	60% (1.8)

Attainment of Cos:

Course Outcome		Direct Attainment	Indirect Attainment	Overall Attainment	Observations
CO1	Describe the floating point and fixed-point arithmetic number representation systems for processing signal in digital signal processor.	0.9	2.3	1.2	Not Attained
CO2	Illustrate the concepts of programmable digital signal processors with control instructions, interrupts and pipeline operations.	0.6	2.4	1	Not Attained
CO3	Demonstrate the instruction sets and addressing modes of TMS320C54XX processor by implementing assembly language programs.	1.6	2.4	1.8	Attained
CO4	Make use of memory and input/output peripherals to interface the programmable DSP devices for increasing time response of a system.	2.3	2.3	2.3	Attained
CO5	Analyze the IIR and FIR filters on programmable digital signal processors using Q15 Format	1.6	2.5	1.8	Attained
CO6	Compute decimation-in time - FFT and decimation-in-frequency - FFT for reducing computational complexity of DFT.	0.9	2.4	1.2	Not Attained

Action Taken Report: (To be filled by the concerned faculty / course coordinator)
CO1: Giving assignments and conducting tutorials on arithmetic number representation systems for processing signal.
CO2: Conducting Guest lectures on programmable digital signal processors for better understanding interrupts and pipeline operations.
CO6: Additional inputs will be provided on decimation-in time - FFT and decimation-in-frequency – FFT for more practice.

Course Coordinator

Mentor

HOD

Head of the Department
Electronics and Communication Engineering
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