INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

ATTAINMENT OF COURSE OUTCOME- ACTION TAKEN REPORT

Name of the Faculty:	Dr. Vijay V	Department:	ECE
Regulation:	IARE-R16	Batch:	2016-2020
Course Name:	Digital System Design	Course Code:	AEC002
Semester:	III	Target Value:	60% (1.8)

Attainment of Cos:

Course Outcome		Direct Attainment	Indirect Attainment	Overall Attainment	Observations
CO1	Outline binary arithmetic operations and optimize boolean functions using karnaugh and tabulation method.	3.00	2.60	2.9	Attained
CO2	Apply combinational circuits for realization of basic building blocks of conventional electronic circuits.	0.90	2.70	1.3	Not attained
CO3	Interpret the knowledge of flip-flops and latches in synchronous and asynchronous modules for memory storing applications.	0.90	2.80	1.3	Not attained
CO4	Extend the logic design techniques for ECL, TTL and CMOS methodologies for designing the fundamental gate level modelling.	0.90	2.60	1.2	Not attained
CO5	Analyze the characteristics of logic families and PLDs to enhance the design skills in digital integrated circuits.	0.60	2.80	1	Not attained
CO6	Evaluate synthesis and simulation of VHDL modules for implementing combinational and sequential circuits for computer aided design tools.	0.60	2.70	1	Not attained

Action Taken Report: (To be filled by the concerned faculty / course coordinator)
In this Course, the CO1, CO2, CO3, CO5 and CO6 requires additional attention and it is improved by

1. Additional inputs will be provided on sum of products and product of sums forms.
2. Additional inputs will be provided on design of combinational circuits using conventional AND, OR, NOT, NAND, NOR and EX-OR gates.
3. Giving assignments and conducting tutorials on karnaugh map representation, minimization using karnaugh map and Quine - McClusky method of minimization.
4. Conducting Guest lectures on Synchronous sequential circuits and shift registers.
5. Conducting Guest lectures on capabilities and limitations of finite state machine.