INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE DESCRIPTION

Course Title	**Switching Theory and Logic Design**			
Course Code	A30407			
Academic Year	2016 - 2017			
Regulation	R15-JNTUH			
Course Structure	**Lectures**	**Tutorials**	**Practicals**	**Credits**
	4	1	-	4
Course Coordinator	Mr. S. Rambabu, Assistant Professor			

I. COURSE OVERVIEW

The course will make them learn the basic theory of switching circuits and their applications in detail. Starting from a problem statement they will learn to design circuits of logic gates that have a specified relationship between signals at the input and output terminals. They will be able to design combinational and sequential circuits .They will learn to design counters, adders, sequence detectors. This course provides a platform for advanced courses like Computer architecture, Microprocessors & Microcontrollers and VLSI design. Greater Emphasis is placed on the use of programmable logic devices and State machines.

II. PREREQUISITE (S)

Level	Credits	Periods / Week	Prerequisites
UG	4	5	Logical Arithmetic

III. MARKS DISTRIBUTION

Sessional Marks	University End Exam Marks	Total Marks
Mid Semester Test There shall be 2 midterm examinations. Each midterm examination consists of subjective type and Objective type tests. The subjective test is for 10 marks, with duration of 1 hour. Subjective test of each semester shall contain 4 questions The student has to answer 2 questions, each carrying 5 marks. The objective type test is for 10 marks with duration of 20minutes. It consists of 10 Multiple choice and 10 objective type questions. The student has to answer all	75	100

the questions and each carries half mark. First midterm examination shall be conducted for the first 21/2 unit of syllabus and second midterm examination shall be conducted for the remaining portion. Five marks are earmarked for assignments. There shall be two assignments in every theory course. Marks shall be awarded considering the average of two assignments in each course reason whatsoever, will get zero marks(s),the conduct of the second mid-examination. The total marks secured by the student in each mid-term examination are evaluated for 25 marks, and the average of the two mid-term examinations shall be taken as the final marks secured by each candidate.		

IV. EVALUATION SCHEME

S. No	Component	Duration (Hrs)	Marks
1	I Mid Examination	1hr 20 min	20
2	I Assignment	--	5
3	II Mid Examination	1hr 20min	20
4	II Assignment	--	5
5	End Semester Examination	3hr	75

V. COURSE EDUCATIONAL OBJECTIVES

1. To learn basic for the design of digital circuits and fundamental concepts used in the design of digital systems.
2. To understand common forms of number representation in digital electronic circuits and to be able to convert between different representations.
3. To implement simple logical operations using combinational logic circuits.
4. To Design combinational logic circuits, sequential logic circuits.
5. To impart to student the concepts of sequential circuits, enabling them to analyze sequential Systems in terms of state machines.
6. To implement synchronous state machines using flip-flops.

VI. COURSE OUTCOMES

1. **Understand** number systems, binary addition and subtraction, 2's complement representation and operations with this representation and understand the different binary codes.
2. **Explain** switching algebra theorems and apply them for logic functions.
3. **Identify** the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.
4. **Discuss** about digital logic gates and their properties.
5. **Evaluate** functions using various types of minimizing algorithms like Boolean algebra, Karnaugh map or tabulation method.
6. **Analyze** the design procedures of Combinational logic circuits.

7. **Understand** bi-stable elements and different types of latches and flip-flops.
8. **Analyze** the design procedures of small sequential circuits and devices and to use standard sequential functions /building blocks to build larger more complex circuits
9. **Understand** and analyze the design a finite state machine, asm charts...

VII. HOW COURSE OUTCOMES ARE ASSESSED

Program Outcomes		Level	Proficiency Assessed by
PO 1	**Engineering Knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	H	Lectures, Assignments, Exercises.
PO 2	**Problem Analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	S	Hands on Practice Sessions.
PO 3	**Design / Development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	N	--
PO 4	**Conduct Investigations of Complex Problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	S	Lab sessions, Exams
PO 5	**Modern Tool Usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	H	Design Exercises.
P0 6	**The Engineer and Society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.	N	--
PO 7	**Environment and Sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.	S	Oral discussions
PO 8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.	N	--
PO 9	**Individual and Team Work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.	H	Seminars Discussions
PO10	**Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.	S	Seminars, Paper Presentations
PO11	**Project Management and Finance**: Demonstrate knowledge and understanding of the engineering and management principles and	S	Discussions, Exams

	apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.		
PO 12	**Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.	**S**	Development of Mini Projects

N - None **S - Supportive** **H - Highly related**

VIII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes		Level	Proficiency Assessed by
PSO 1	**Professional Skills:** Able to utilize the knowledge of high voltage engineering in collaboration with power systems in innovative, dynamic and challenging environment, for the research based team work.	H	Lectures and Assignments
PSO 2	**Problem-Solving Skills:** Can explore the scientific theories, ideas, methodologies and the new cutting edge technologies in renewable energy engineering, and use this erudition in their professional development and gain sufficient competence to solve the current and future energy problems universally.	S	Tutorials
PSO 3	**Successful Career and Entrepreneurship:** The understanding of technologies like PLC, PMC, process controllers, transducers and HMI one can analyze, design electrical and electronics principles to install, test , maintain power system and applications.	S	Seminars and Projects

N - None **S - Supportive** **H – Highly Related**

IX. SYLLABUS:

UNIT -I:Number System and Boolean Algebra And Switching Functions:
Number Systems, Base Conversion Methods, Complements of Numbers, Codes- Binary Codes, Binary Coded Decimal Code and its Properties, Unit Distance Codes, Alpha Numeric Codes, Error Detecting and Correcting Codes.
Boolean Algebra: Basic Theorems and Properties, Switching Functions, Canonical and Standard Form, Algebraic Simplification of Digital Logic Gates, Properties of XOR Gates, Universal Gates, Multilevel NAND/NOR realizations.

UNIT –II: Minimization and Design of Combinational Circuits:
Introduction, The Minimization with theorem, The Karnaugh Map Method, Five and Six Variable Maps, Prime and Essential Implications, Don't Care Map Entries, Using the Maps for Simplifying, Tabular Method, Partially Specified Expressions, Multi-output Minimization, Minimization and Combinational Design, Arithmetic Circuits, Comparator, Multiplexers, Code Converters, Wired Logic, Tristate Bus System, Practical Aspects related to Combinational Logic Design, Hazards and Hazard Free Relations.

UNIT -III: Sequential Machines Fundamentals:

Introduction, Basic Architectural Distinctions between Combinational and Sequential circuits, The Binary Cell, Fundamentals of Sequential Machine Operation, The Flip-Flop, The D-Latch Flip-Flop, The "Clocked T" Flip-Flop, The " Clocked J-K" Flip-Flop, Design of a Clocked Flip-Flop, Conversion from one type of Flip-Flop to another, Timing and Triggering Consideration, Clock Skew.

UNIT -IV: Sequential Circuit Design and Analysis:

Introduction, State Diagram, Analysis of Synchronous Sequential Circuits, Approaches to the Design of Synchronous Sequential Finite State Machines, Design Aspects, State Reduction, Design Steps, Realization using Flip-Flops

Counters - Design of Single mode Counter, Ripple Counter, Ring Counter, Shift Register, Shift Register Sequences, Ring Counter Using Shift Register.

UNIT -V:

Sequential Circuits: Finite state machine-capabilities and limitations, Mealy and Moore models-minimization of completely specified and incompletely specified sequential machines, Partition techniques and Merger chart methods-concept of minimal cover table.

Algorithmic State Machines: Salient features of the ASM chart-Simple examples-System design using data path and control subsystems-control implementations-examples of Weighing machine and Binary multiplier.

TEXTBOOKS:

1. M Morris Mano, Michael D. Ciletti (2008), *Digital Design*, 3rd edition, Pearson Education/PHI, India.
2. Zvi Kohavi (2004), Switching and Finite Automata Theory, 3rd edition, Tata McGraw Hill, India

REFERENCE BOOKS:

1. Fredriac J. Hill, Gerald R.Peterson, 3rd edition, Introduction to switching theory and logic design.
2. Thomas L.Floyd , Pearson 2013, Digital fundamentals – A Systems Approach
3. Ye Brian and Holds Worth, Elsevier, Digital logic design
4. John M. Yarbrough, Thomson publications 2006tld syllabus, Digital logic applications and design.
5. Roth (2004), Fundamentals of Logic Design, 5th edition, Thomson.
6. Comer, 3rd, oxford 2013, Digital Logic and State machine Design
7. Anand Kumar, Switching Theory and Logic Design

X. COURSE PLAN

At the end of the course, the students are able to achieve the following course learning outcomes (CLO):

Lecture No.	Unit No	Topics to be covered	Course Learning Outcomes	Reference
1-3	I	Number systems, base conversion methods	**Understand** the different number systems and its conversions.	T1 - 1.1 to 1.5
4-5		Complements of numbers codes-binary codes, BCD code and its properties ,	**Understand** the arithmetic operations carried by digital systems.	T1 - 1.7
6-7		Unit distance code, alphanumeric codes, and error detecting and correcting codes.	**Understand** the different code representations in digital systems.	T1 - 1.7
8-10		Basic theorems and its properties, switching functions, canonical and standard form.	**Learn** Boolean algebra and logical operations in Boolean algebra.	T1 – 2.1 to 2.6
11-13		Algebraic simplification of digital logic gates, properties of XOR gates.	**Apply** different logic gates to functions and simplify them.	T1 – 2.8
14-15		Universal gates, Multilevel NAND/NOR realizations.	**Understand** and build the different functions by using universal gates.	T1- 3.7 to 3.8
16-21	II	Introduction, the minimization with theorem , The k-map method, five and six -variable map Prime and essential implications, Don't care map entries, using K maps for simplifying	**Analyze** the redundant terms and minimize the expression using K-maps	T1 - 3.1 to 3.9
22-23	II	Tabular method, Partially specified expressions , multi-output minimization	**Identify** the redundant terms and minimize the expression using tabular method	T1 - 3.5 to 3.9
24-26		combinational design, arithmetic circuits, comparator, multiplexers	**Apply** the logic gates and design of combinational circuits	T1 – 4.1 to 4.9
27-31		Code convertors, wired logic, tristate bus system, practical aspects related to combinational logic design, hazards and hazard free relations.	**Design** of different combinational logic circuits	R4 - 6.4.3 , 4.11
32-33	III	Introduction**,** Basic architectural distinctions between combinational and sequential circuits, the binary cell, the fundamentals of sequential machine operation.	**Understand** the clock dependent circuits and identify the differences between clocked and clock less circuits	T1 – 5.1 to 5.2

34-36		flip-flop, D-Latch Flip-flop, "Clocked T" Flip-flop, "Clocked JK " flip-flop. design of a clocked flip-flop conversion from one type of flip-flop to another	**Apply** and design clock dependent circuits.	T1 – 5.3 to 5.5
37		Timing and triggering consideration , clock skew	**Understand** how the flip-flops are synchronized.	T1 - 5.5
38-39	IV	Introduction, State diagrams, Analysis of synchronous sequential circuit	**Understand** how synchronous sequential circuit works.	T1 - 5.7 to 5.8
40-45	IV	Approaches to the design of synchronous sequential finite state machines, design aspects State reduction, design steps, realization using flip-flop.	**Analyze** the procedure to reduce the internal states in sequential circuits.	T1 - 6.1, 6.3
46-49		Ripple counter, Ring counter, Shift registers, Shift register sequences, Ring counter using shift register.	**Apply** the sequential circuits and design the different memory devices and counting circuits.	T1 - 6.1 to 6.5
50-51	V	Finite State machine – Capabilities and limitations, mealy and Moore models.	**Understand** the FSM and its design principles.	R4 - 7.1 to 7.2
52-58		Minimization of completely specified and incompletely specified sequential machines partition techniques and merger chart methods – concept of minimal cover table.	**Illustrate** minimization of complete and incomplete state machines and to write a minimal cover table.	R4 - 7.3, 7.4
59-62		Salient features of the ASM Chart- Simple Examples-system design using data path and control subsystems	**Model** an ASM chart and describe system design using different techniques.	R4 - 7.5, 7.7
63-65		control implementations	**Illustrate** control implementations	R7
	V	Examples of weighing machine and Binary multiplier	**Analyze** the different examples to ASM.	R5 - 18.1 TO 18.3

XI. MAPPING COURSE OBJECTIVES LEADING TO THE ACHIEVEMENT OF THE PROGRAM OUTCOMES

Course Objectives	Program Out Comes												PSO		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
I	H			H	H						S	S			
II		S	H		S				H						
III					S				H						
IV			S						H						
V	S	H			H							S			
VI	H			H	H						S	S			

S = Supportive **H = Highly Related**

XI: MAPPING COURSE LEARNING OBJECTIVES LEADING TO THE ACHIEVEMENT OF THE PROGRAM OUTCOMES:

Course Outcomes	PROGRAM OUTCOMES											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11	PO 12
1	S	S							H			S
2	S	H	S						S	S		
3	H	H	S	S					S			
4	H	H	H	S	S				S	S		S
5	H	S	S						S			
6	H	S	H	H			S		S	S		H
7	S	H	H	S	S				S		S	S
8	S	S	H	S	S		S		S		S	S
9	H	H			S				S		H	H

S = Supportive **H = Highly Related**

Prepared By: S. Rambabu, Assistant Professor

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