INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTION

Course Title	**SWITCHING THEORY AND LOGIC DESIGN**			
Course Code	**A30407**			
Course Structure	**Lectures**	**Tutorials**	**Practicals**	**Credits**
	4	1	-	4
Course Coordinator	Mr .B. Naresh, Assistant Professor			
Team of Instructors	Ms Kalyani, Assistant Professor			

I. Course overview

The course will make them learn the basic theory of switching circuits and their applications in detail. Starting from a problem statement they will learn to design circuits of logic gates that have a specified relationship between signals at the input and output terminals. They will be able to design combinational and sequential circuits .They will learn to design counters, adders, sequence detectors. This course provides a platform for advanced courses like Computer architecture, Microprocessors & Microcontrollers and VLSI design. Greater Emphasis is placed on the use of programmable logic devices and State machines.

II. Prerequisite(s)

Level	Credits	Periods / Week	Prerequisites
UG	4	5	Logical Arithmetic

III. Marks Distribution

Sessional Marks	University End Exam marks	Total marks
Mid Semester Test There shall be 2 midterm examinations. Each midterm examination consists of subjective type and Objective type tests. The subjective test is for 10 marks, with duration of 1 hour. Subjective test of each semester shall contain 4 questions The student has to answer 2 questions, each carrying 5 marks. The objective type test is for 10 marks with duration of 20minutes. It consists of 10 Multiple choice and 10 objective type questions. The student has to answer all the questions and each carries half mark. First midterm examination shall be conducted for the first 21/2 unit of syllabus and second midterm examination shall be conducted for the remaining portion. Five marks are earmarked for assignments. There shall be two assignments in every theory course. Marks shall be awarded considering the average of two assignments in each course reason whatsoever, will get zero marks(s).the conduct of the second mid-examination. The total marks secured by the student in each mid-term examination are evaluated for 25 marks, and the average of the	75	100

two mid-term examinations shall be taken as the final marks secured by each candidate.		

IV. Evaluation Scheme

Sl.No	Component	Duration(Hrs)	Marks
1	I Mid Examination	1hr 20 min	20
2	I Assignment	--	5
3	II Mid Examination	1hr 20min	20
4	II Assignment	--	5
5	End Semester Examination	3hr	75

V. Course Educational Objectives

1. To learn basic for the design of digital circuits and fundamental concepts used in the design of digital systems.
2. To understand common forms of number representation in digital electronic circuits and to be able to convert between different representations.
3. To implement simple logical operations using combinational logic circuits.
4. To Design combinational logic circuits, sequential logic circuits.
5. To impart to student the concepts of sequential circuits, enabling them to analyze sequential Systems in terms of state machines.
6. To implement synchronous state machines using flip-flops.

VI. Course Outcomes

1. **Understand** number systems, binary addition and subtraction, 2's complement representation and operations with this representation and understand the different binary codes.
2. **Explain** switching algebra theorems and apply them for logic functions.
3. **Identify** the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.
4. **Discuss** about digital logic gates and their properties.
5. **Evaluate** functions using various types of minimizing algorithms like Boolean algebra, Karnaugh map or tabulation method.
6. **Analyze** the design procedures of Combinational logic circuits.
7. **Understand** bi-stable elements and different types of latches and flip-flops.
8. **Analyze** the design procedures of small sequential circuits and devices and to use standard sequential functions /building blocks to build larger more complex circuits
9. **Understand** and analyze the design a finite state machine, asm charts...

VII. How Course Outcomes are assessed

Program Outcomes		Level	Proficiency assessed by
PO 1	**Engineering knowledge**: An ability to apply knowledge of basic sciences, mathematical skills, engineering and technology to solve complex electronics and communication engineering problems (**Fundamental Engineering Analysis Skills**).	**H**	Lectures, Assignments, Exercises.
PO 2	**Problem analysis**: An ability to identify, formulate and analyze engineering problems using knowledge of Basic Mathematics and Engineering Sciences (**Engineering Problem Solving**	**S**	Hands on Practice Sessions.

	Skills).		
PO 3	**Design/development of solutions**: An ability to provide solution and to design Electronics and Communication Systems as per social needs **(Social Awareness).**	**N**	--
PO 4	**Conduct investigations of complex problems**: An ability to investigate the problems in Electronics and Communication field and develop suitable solutions (**Creative Skills**).	**S**	Lab sessions, Exams
PO 5	**Modern tool usage:** An ability to use latest hardware and software tools to solve complex engineering problems (**Software and Hardware Interface**).	**H**	Design Exercises.
P0 6	**The engineer and society**: An ability to apply knowledge of contemporary issues like health, Safety and legal which influences engineering design **(Social Awareness).**	**N**	--
PO 7	**Environment and sustainability**: An ability to have awareness on society and environment for sustainable solutions to Electronics and Communication Engineering problems **(Social Awareness).**	**S**	Oral discussions
PO 8	**Ethics**: An ability to demonstrate understanding of professional and ethical responsibilities **(Professional Integrity).**	**N**	--
PO 9	**Individual and team work**: An ability to work efficiently as an individual and in multidisciplinary teams **(Team work).**	**H**	Seminars Discussions
PO 10	**Communication**: An ability to communicate effectively and efficiently both in verbal and written form **(Communication Skills).**	**S**	Seminars, Paper Presentations
PO 11	**Life-long learning**: An ability to develop confidence to pursue higher education and for life-long learning **(Continuing Education Awareness).**	**S**	Discussions, Exams
PO 12	**Project management and finance**: An ability to design, implement and manage the electronic projects for real world applications with optimum financial resources **(Practical Engineering Analysis Skills**).	**S**	Development of Mini Projects

N - None **S - Supportive** **H - Highly related**

VIII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

PROGRAM SPECIFIC OUTCOMES		LEVEL	PROFICIENCY ASSESSED BY
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	H	Lectures and Assignments
PSO 2	**Problem-solving skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	S	Tutorials
PSO 3	**Successful career and Entrepreneurship:** An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.	S	Seminars and Projects

N - None **S - Supportive** **H – Highly Related**

IX. Syllabus:

UNIT -I:Number System and Boolean Algebra And Switching Functions:
Number Systems, Base Conversion Methods, Complements of Numbers, Codes- Binary Codes, Binary Coded Decimal Code and its Properties, Unit Distance Codes, Alpha Numeric Codes, Error Detecting and Correcting Codes.
Boolean Algebra: Basic Theorems and Properties, Switching Functions, Canonical and Standard Form, Algebraic Simplification of Digital Logic Gates, Properties of XOR Gates, Universal Gates, Multilevel NAND/NOR realizations.

UNIT –II: Minimization and Design of Combinational Circuits:
Introduction, The Minimization with theorem, The Karnaugh Map Method, Five and Six Variable Maps, Prime and Essential Implications, Don't Care Map Entries, Using the Maps for Simplifying, Tabular Method, Partially Specified Expressions, Multi-output Minimization, Minimization and Combinational Design, Arithmetic Circuits, Comparator, Multiplexers, Code Converters, Wired Logic, Tristate Bus System, Practical Aspects related to Combinational Logic Design, Hazards and Hazard Free Relations.

UNIT -III: Sequential Machines Fundamentals:
Introduction, Basic Architectural Distinctions between Combinational and Sequential circuits, The Binary Cell, Fundamentals of Sequential Machine Operation, The Flip-Flop, The D-Latch Flip-Flop, The "Clocked T" Flip-Flop, The " Clocked J-K" Flip-Flop, Design of a Clocked Flip-Flop, Conversion from one type of Flip-Flop to another, Timing and Triggering Consideration, Clock Skew.

UNIT -IV: Sequential Circuit Design and Analysis:
Introduction, State Diagram, Analysis of Synchronous Sequential Circuits, Approaches to the Design of Synchronous Sequential Finite State Machines, Design Aspects, State Reduction, Design Steps, Realization using Flip-Flops
Counters - Design of Single mode Counter, Ripple Counter, Ring Counter, Shift Register, Shift Register Sequences, Ring Counter Using Shift Register.

UNIT -V:

Sequential Circuits: Finite state machine-capabilities and limitations, Mealy and Moore models-minimization of completely specified and incompletely specified sequential machines, Partition techniques and Merger chart methods-concept of minimal cover table.

Algorithmic State Machines: Salient features of the ASM chart-Simple examples-System design using data path and control subsystems-control implementations-examples of Weighing machine and Binary multiplier.

Textbooks:

1. M. Morris Mano, Michael D. Ciletti (2008), *Digital Design*, 3rd edition, Pearson Education/PHI, India.
2. Zvi. Kohavi (2004), Switching and Finite Automata Theory, 3rd edition, Tata McGraw Hill, India

Reference Books:

1. Fredriac J. Hill, Gerald R.Peterson, 3rd edition, Introduction to switching theory and logic design.
2. Thomas L.Floyd , Pearson 2013, Digital fundamentals – A Systems Approach
3. Ye Brian and Holds Worth, Elsevier, Digital logic design
4. John M. Yarbrough, Thomson publications 2006tld syllabus, Digital logic applications and design.
5. Roth (2004), Fundamentals of Logic Design, 5th edition, Thomson.
6. Comer, 3rd, oxford 2013, Digital Logic and State machine Design
7. Anand Kumar, Switching Theory and Logic Design

X. Course Plan

At the end of the course, the students are able to achieve the following course learning outcomes (CLO):

Lecture No.	Unit NO	Topics to be covered	Course Learning Outcomes	Reference
1-3	I	Number systems, base conversion methods.	**Understand** the different number systems and its conversions.	T1 - 1.1 to 1.5
4-6		Complements of numbers, codes-binary codes, BCD code and its properties.	**Understand** the arithmetic operations carried by digital systems.	T1 - 1.7
7-8		Unit distance code, alphanumeric codes, and error detecting and correcting codes.	**Understand** the different code representations in digital systems.	T1 - 1.7
9-11		Basic theorems and its properties, switching functions, canonical and standard form.	**Learn** Boolean algebra and logical operations in Boolean algebra.	T1 – 2.1 to 2.6
12-14		Algebraic simplification of digital logic gates, properties of XOR gates.	**Apply** different logic gates to functions and simplify them.	T1 – 2.8
15-16		Universal gates, Multilevel NAND/NOR realizations.	**Understand** and build the different functions by using universal gates.	T1- 3.7 to 3.8
17-21	II	Introduction, the minimization with theorem, The k-map method, five and six -variable map Prime and essential implications Don't care map entries, using K maps for simplifying.	**Analyze** the redundant terms and minimize the expression using K-maps	T1 - 3.1 to 3.9
22-24		Tabular method, Partially specified expressions, multi-output minimization.	**Identify** the redundant terms and minimize the expression using tabular method	T1 - 3.5 to 3.9

25-27	II	combinational design, arithmetic circuits, comparator, multiplexers	**Apply** the logic gates and design of combinational circuits	T1 – 4.1 to 4.9
28-32		Code convertors, wired logic, tristate bus system, practical aspects related to combinational logic design, hazards and hazard free realizations.	**Design** of different combinational logic circuits	R4 - 6.4.3 , 4.11
33-34	III	Introduction**,** Basic architectural distinctions between combinational and sequential circuits, the binary cell, the fundamentals of sequential machine operation.	**Understand** the clock dependent circuits and identify the differences between clocked and clock less circuits	T1 – 5.1 to 5.2
35-37		Flip-flop, D-Latch Flip-flop, "Clocked T" Flip-flop, "Clocked JK "flip-flop. design of a clocked flip-flop conversion from one type of flip-flop to another.	**Apply** and design clock dependent circuits.	T1 – 5.3 to 5.5
38		Timing and triggering consideration, clock skew.	**Understand** how the flip-flops are synchronized.	T1 - 5.5
39-40	IV	Introduction, State diagrams, Analysis of synchronous sequential circuit.	**Understand** how synchronous sequential circuit works.	T1 - 5.7 to 5.8
41-45		Approaches to the design of synchronous sequential finite state machines, design aspects State reduction, design steps, realization using flip-flop.	**Analyze** the procedure to reduce the internal states in sequential circuits.	T1 - 6.1, 6.3
46-50		Design of single mode counter, Ripple counter, Ring counter, Shift registers, Shift register sequences, Ring counter using shift register.	**Apply** the sequential circuits and design the different memory devices and counting circuits.	T1 - 6.1 to 6.5
51-52	V	Finite State machine – Capabilities and limitations, mealy and Moore models.	**Understand** the FSM and its design principles.	R4 - 7.1 to 7.2
53-59		Minimization of completely specified and incompletely specified sequential machines, partition techniques and merger chart methods – concept of minimal cover table.	**Illustrate** minimization of complete and incomplete state machines and to write a minimal cover table.	R4 - 7.3, 7.4
60-63		Salient features of the ASM Chart- Simple Examples- system design using data path and control subsystems	**Model** an ASM chart and describe system design using different techniques.	R4 - 7.5, 7.7
64		control implementations	**Illustrate** control implementations	R7
65-66		Examples of weighing machine and Binary multiplier	**Analyze** the different examples to ASM.	R5 - 18.1 TO 18.3

XI: Mapping course objectives leading to the achievement of the program outcomes

Course Objectives	Program Out Comes												Program Specific Outcomes		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
I	H			H	H						S	S	H		
II		S	H		S				H				H	S	
III					S				H				S	H	
IV			S						H				S	H	S
V	S	H			H							S	H	S	S
VI	H			H	H						S	S	S	H	S

S = Supportive H = Highly Related

XII: Mapping course learning objectives leading to the achievement of the program outcomes:

Course Outcomes	PROGRAM OUTCOMES												Program Specific Outcomes		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
1	S	S							H			S	S	S	
2	S	H	S						S	S			S	S	
3	H	H	S	S					S				S		
4	H	H	H	S	S				S	S		S	S		
5	H	S	S						S				S	H	
6	H	S	H	H			S		S	S		H	S	S	S
7	S	H	H	S	S				S		S	S	S	S	S
8	S	S	H	S	S		S		S		S	S	H	S	S
9	H	H			S				S		H	H	S	S	

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