INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

COMPUTER SCIENCE AND ENGINEERING

COURSE DESCRIPTOR

Course Title	COMPUTER ORGANIZATION AND ARCHITECTURE				
Course Code	ACSB07				
Programme	B.Tech				
Semester	IV	CSE	IT		
Course Type	Core				
Regulation	IARE – R18				
Course Structure	**Theory**			**Practical**	
	Lectures	Tutorials	Credits	Laboratory	Credits
	3	-	3	-	-
Chief Coordinator	Mr. E Sunil Reddy, Assistant Professor				
Course Faculty	Dr.P.L.Srinivasa Murthy. Professor Mr. N Rajasekhar, Assistant Professor Ms. B.DhanaLaxmi, Assistant Professor				

I. COURSEOVERVIEW:

This course introduces the principles of basic computer organization, CPU organization, and the basic architecture concepts. The course emphasizes performance and cost analysis, instruction set design, register transfer languages, arithmetic, logic and shift micro operations, pipelining, memory technology, memory hierarchy, virtual memory management, and I/O organization of computer, parallel processing and inter process communication and synchronization. This course in reached to student by power point presentations, lecture notes, and assignment questions, previous model question papers, multiple choice questions and question bank of long and short answers.

II. COURSEPRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
-	-	-	-	-

III. MARKSDISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Computer Organization and Architecture	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONALMETHODOLOGIES:

✘	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATIONMETHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of theconcept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 20 marks for Continuous Internal Examination (CIE), 05 marks for Quiz and 05 marks for Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	Theory			Total Marks
Type of Assessment	CIE Exam	Quiz	AAT	
CIA Marks	20	05	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 8th and 16thweek of the semester respectively. The CIE exam is conducted for 20 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIEexams.

Quiz -Online Examination
Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are to be answered by choosing the correct answer from a given set of choices (commonly four). Such a question paper shall be useful in testing of knowledge, skills, application, analysis, evaluation and understanding of the students. Marks shall be awarded considering the average of two quiz examinations for every course.

Alternative Assessment Tool (AAT):
This AAT enables faculty to design own assessment patterns during the CIA. The AAT converts the classroom into an effective learning Centre. The AAT may include tutorial hours/classes, seminars,

assignments, term paper, open ended experiments, METE (Modeling and Experimental Tools in Engineering), five minutes video, MOOCs etc.

VI. HOW PROGRAM OUTCOMES AREASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Presentation on real-world problems
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences	2	Assignment
PO 3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified need switch appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations	2	Seminar

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES AREASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** The ability to understand, analyze and develop computer programs in the areas related to algorithms, system software, multimedia, web design, big data analytics, and networking for efficient design of computer-based systems of varying complexity.	1	Seminar
PSO 2	**Problem-Solving Skills:** The ability to apply standard practices and strategies in software project development using open-ended programming environments to deliver a quality product for business success	-	-
PSO 3	**Successful Career and Entrepreneurship:** The ability to employ modern computer languages, environments, and platforms in creating innovative career paths to be an entrepreneur, and a zest for higher studies.	-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES:

The course should enable the students to:	
I	Understand the organization and architecture of computer systems and electronic computers.
II	Study the assembly language program execution, instruction format and instruction cycle.
III	Design a simple computer using hardwired and micro programmed control methods.
IV	Study the basic components of computer systems besides the computer arithmetic
V	Understand input-output organization, memory organization and management, and pipelining.

IX. COURSE OUTCOMES(COs):

Cos	Course Outcome	CLOs	At the end of the course, the student will have the ability to:
CO 1	Understand the organization and levels of design in computer architecture and To understand the concepts of programming methodologies.	CLO 1	Describe the various components like input/output units, memory unit, control unit, arithmetic logic unit connected in the basic organization of a computer.
		CLO 2	Understand the interfacing concept with memory subsystem organizationand input/output subsystemorganization.
		CLO 3	Understand instruction types, addressing modes and their formats in the assembly language programs.
CO 2	Describe Register transfer languages, arithmetic micro operations, logic micro operations, shift micro operations address sequencing, micro program example, and design of control unit.	CLO 4	Describe the instruction set architecture design for relatively simple microprocessor or Central Processing Unit.
		CLO 5	Classify the functionalities of various micro operations such as arithmetic, logic and shift micro operations.
		CLO 6	Understand the register transfer languages and micro operations involved in bus and memory transfers.
CO 3	Understand the Instruction cycle, data representation, memory reference instructions, input-output, and interrupt, addressing modes, data transfer and manipulation, program control. Computer arithmetic: Addition and subtraction, floating point arithmetic operations, decimal arithmetic unit.	CLO 7	Describe the design of control unit with address sequencing and microprogramming Concepts
		CLO 8	Understand the connections among the circuits and the Functionalities in the hardwired control unit
		CLO 9	Describe the various phases involved in the instruction cycle viz. fetching, decoding, reading effective address and execution of instruction.
		CLO 10	Understand the different priority interrupts in the input-output organization in the computerarchitecture.
CO 4	Knowledge aboutMemory hierarchy, main memory, auxiliary memory, associative memory, cache memory, virtual memory Input or output Interface, asynchronous data transfer, modes of transfer, priority interrupt, direct memory access.	CLO 11	Describe various data representations and explain how arithmetic and logical operationsare performed by computers.
		CLO 12	Classify the various instructions formats to solve the arithmetic expressions in different addressing modes.
		CLO 13	Understand the functionality of various instruction formats for writing assembly language programs.
		CLO 14	Describe the hardware organization of associate memory and understand the read and write operation
CO 5	Explore the Parallel processing, pipelining-arithmetic pipeline, instruction pipeline Characteristics of multiprocessors, inter connection structures, inter processor arbitration, inter processor Communication and synchronization .	CLO 15	Describe the implementation of fixed point and floating point addition, subtraction operations.
		CLO 16	Understand the concept of memory hierarchy and different typed of memory chips.
		CLO 17	Describe various modes of data transfer between CPU and I/O devices
		CLO 18	Understand the virtual memory concept with page replacement concept in memory organization
		CLO 19	Describe the parallel processing concept with multiple functional units.
		CLO 20	Understand the multiprocessor concept with system bus structure and the concept of inter processor communication and synchronization.

X. COURSE LEARNING OUTCOMES(CLOs):

CLOCode	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
ACSB07.01	CLO 1	Describe the various components like input/output units, memory unit, control unit, arithmetic logic unit connected in the basic organization of a computer.	PO 1	3
ACSB07.02	CLO 2	Understand the interfacing concept with memory subsystem organizationand Input/output subsystemorganization.	PO 1	3
ACSB07.03	CLO 3	Understand instruction types, addressing modes and their formats in the assemblylanguage programs.	PO 2	2
ACSB07.04	CLO 4	Describe the instruction set architecturedesign for relatively simple microprocessor or Central Processing Unit.	PO 3	1
ACSB07.05	CLO 5	Classify the functionalities of various micro operations such as arithmetic, logic and shift micro operations.	PO 3	2
ACSB07.06	CLO 6	Understand the register transfer languagesand micro operations involved in bus and memory transfers.	PO 2	2
ACSB07.07	CLO 7	Describe the design of control unit withaddress sequencing and microprogramming Concepts.	PO3	1
ACSB07.08	CLO 8	Understand the connections among thecircuits and the functionalities in the hardwired control unit.	PO2	1
ACSB07.09	CLO 9	Describe the various phases involved in the instruction cycle viz. fetching, decoding, reading effective address and execution ofinstruction.	PO 2	3
ACSB07.10	CLO 10	Describe various data representations and explain how arithmetic and logical operations are performed by computers.	PO 2	1
ACSB07.11	CLO 11	Classify the various instructions formats tosolve the arithmetic expressions in different addressing modes.	PO1	1
ACSB07.12	CLO 12	Understand the functionality of various instruction formats for writing assemblylanguage programs.	PO 2	1
ACSB07.13	CLO 13	Describe the implementation of fixed pointand floating point addition, subtraction operations.	PO 1	3
ACSB07.14	CLO 14	Understand the concept of memory hierarchy and different typed of memory chips.	PO 2	2
ACSB07.15	CLO 15	Describe various modes of data transferbetween CPU and I/O devices	PO2, PO3	1
ACSB07.16	CLO 16	Understand the virtual memory concept with page replacement concept in memory organization	PO 2	2
ACSB07.17	CLO 17	Describe the hardware organization of associate memory and understand the readand write operations	PO1, PO2	1
ACSB07.18	CLO 18	Describe the parallel processing concept with multiple functional units.	PO 2	2

ACSB07.19	CLO 19	Understand the multiprocessor concept with system bus structure and the concept of inter processor communication andsynchronization.	PO 1	2
ACSB07.20	CLO 20	Understand the different priority interrupts in the input-output organization in the computer architecture.	PO 1	2
ACSB07.21	CLO 21	Possess the knowledge and skills for employability and to succeed in nationaland international level competitiveexaminations.	PO 2	1
ACSB07.22	CLO 22	Possess the knowledge and skills to design advanced computer architecture for current industry requirements.	PO 1	1

3 = High; 2 = Medium; 1 = Low

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFICOUTCOMES:

Course Outcomes (COs)	Program Outcomes(POs)			Program Specific Outcomes (PSOs)
	PO 1	PO2	PO3	PSO 1
CO 1	3	1		1
CO 2		2	2	2
CO 3		2	1	1
CO 4	2	1		2
CO 5	2	1	1	2

3 = High; 2 = Medium; 1 = Low

XII. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFICOUTCOMES:

(CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3												1		
CLO 2	3												1		
CLO 3		2													
CLO 4			1										1		
CLO 5			2										1		
CLO 6		2											1		
CLO 7			2												
CLO 8		2											1		
CLO 9		3													
CLO 10		1											1		

CLO 11	2												1		
CLO 12		1													
CLO 13	3												1		
CLO 14		2											1		
CLO 15		1	2										1		
CLO 16		2													
CLO 17	2	1											1		
CLO 18		2													
CLO 19	2												1		
CLO 20	2												1		
CLO 21		1													
CLO 22	1														

3 = High; 2 = Medium; 1 = Low

XIII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO 1,PO2, PO 3, PSO1	SEE Exams	PO 1,PO2, PO 3, PSO1	Assignments	PO 2	Seminars	PO 3
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	-						

XIV. ASSESSMENT METHODOLOGIES -INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XV. SYLLABUS

MODULE-I	INTRODUCTION TO COMPUTER ORGANIZATION
Basic computer organization, CPU organization, memory subsystem organization and interfacing, input or output subsystem organization and interfacing, a simple computer levels of programming languages, assembly language instructions, instruction set architecture design, a simple instruction set architecture.	
MODULE-II	ORGANIZATION OF A COMPUTER
Register transfer: Register transfer language, register transfer, bus and memory transfers, arithmetic micro operations, logic micro operations, shift micro operations; Control unit: Control memory, address sequencing, micro program example, and design of control unit.	
MODULE-III	CPU AND COMPUTER ARITHMETIC
CPU design: Instruction cycle, data representation, memory reference instructions, input-output, and interrupt, addressing modes, data transfer and manipulation, program control. Computer arithmetic: Addition and subtraction, floating point arithmetic operations, decimal arithmetic unit.	
MODULE-IV	INPUT-OUTPUT ORGANIZATION AND MEMORY ORGANIZATION

	Memory organization: Memory hierarchy, main memory, auxiliary memory, associative memory, cache memory, virtual memory; Input or output organization: Input or output Interface, asynchronous data transfer, modes of transfer, priority interrupt, direct memory access.
MODULE-V	**MULTIPROCESSORS**

Pipeline: Parallel processing, pipelining-arithmetic pipeline, instruction pipeline; Multiprocessors: Characteristics of multiprocessors, inter connection structures, inter processor arbitration, inter processor communication and synchronization.

Text Books:

1. M. Morris Mano, —"Computer Systems Architecture", Pearson, 3rd Edition,2007.
2. John D. Carpinelli, —"Computer Systems Organization and Architecture", Pearson, 1st Edition, 2001.
3. Patterson, Hennessy, —"Computer Organization and Design: the Hardware/Software nterface", Morgan Kaufmann, 5th Edition,2013.

Reference Books:

1. John. P. Hayes, —"Computer System Architecture", McGraw-Hill, 3rd Edition,1998.
2. Carl Hamacher, Zvonko G Vranesic, SafwatGZaky, —"Computer Organization", McGraw-Hill, 5th Edition,2002.
3. William Stallings, —"Computer Organization and Architecture", Pearson Edition, 8th Edition,2010.

XVI. COURSEPLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1	Basic Computer Organization	CLO 1	T1: 4.1-4.2
2-4	Memory Subsystem Organization And Interfacing, Input Or Output Subsystem Organization And Interfacing	CLO 2	T1: 4.3-4.4
5-7	Computer Levels Of Programming Languages, AssemblyLanguage Instructions	CLO 3	T1: 3.1-3.2
8-12	Instruction Set Architecture Design, A Simple Instruction Set Architecture	CLO 4	T1: 3.3-3.4
13-15	Arithmetic Micro Operations, Logic Micro Operations	CLO 5	T2: 4.4-45
16-19	Control Unit: Control Memory, Address Sequencing	CLO 7	T2: 7.1-7.2
20-22	Design Of Control Unit	CLO 7	T2: 7.4
23	Data Representation	CLO 10	T2: 3.1-3.3
24-26	Memory Reference Instructions, Input- Output, And Interrupt	CLO 11	T2: 5.6-5.7
27-32	Addressing Modes, Program Control	CLO 11	T2: 8.5-8.7
33-35	Memory Reference Instructions, Data Transfer And Manipulation	CLO 12	T2: 8.6
36-38	Computer Arithmetic: Addition And Subtraction, Floating Point Arithmetic Operations	CLO 13	T2: 10.1-10.5
39-42	Memory Organization	CLO 14	T2: 12.1
43-45	Input Or Output Interface	CLO 15	T2: 11.2
46-48	Asynchronous Data Transfer, Modes Of Transfer	CLO 17	T2: 11.3-11.4
49	Priority Interrupt	CLO 20	T2: 11.5

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
50-51	Direct Memory Access	CLO 17	T2: 11.6
52-53	Pipeline: Parallel Processing	CLO 18	T2: 9.1-9.2
54	Instruction Pipeline	CLO 19	T2: 9.4
55-56	Multiprocessors	CLO 19	T2: 13.1
57-58	Inter Connection Structures	CLO 19	T2: 13.2
59-60	Inter Processor Arbitration	CLO 19	T2: 13.3

XVII. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSIONREQUIREMENTS:

S No	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	Data Representation – Arithmetic multiplication , division	Seminars / Guest Lectures/ NPTEL	PO 1	PSO 1
2	RISC ,CISC Characteristics	Seminars / Guest Lectures/ NPTEL	PO 2	PSO 1
3	Vector Processing	Assignments	PO 1	PSO 1

Prepared by:

Mr. E Sunil Reddy, Assistant Professor

HOD, CSE