Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC020

INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)

B.Tech III Semester End Examinations (Regular) - December, 2017

Regulation: IARE – R16

DIGITAL LOGIC DESIGN
(Common to CSE / IT)

Time: 3 Hours **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Perform the subtraction with the following decimal numbers by taking the 10's complement of the subtrahend. **[6M]**
   i. 20-100
   ii. 1753-8640
   (b) Convert the decimal 153 to octal and (0.6875)10 to binary, clearly indicate each step during the process of conversion. **[8M]**
2. (a) Illustrate the process of detecting errors during the transmission of information from one location to another using parity bits. **[7M]**
   (b) What is Radix complement? Explain the procedure of complementing r of an n-digit number N in base r. **[7M]**

UNIT – II

3. (a) Convert the following expressions into sum of products and product of sums: **[5M]**
   i. (AB+C)(B+C'D)
   ii. x' + x(x+y') (y+z')
   (b) Simplify the following Boolean functions by first finding the essential prime implicants: **[9M]**
   i. F(w, x, y, z) = $\sum$m(0,2,4,5,6,7,8,10,13,15)
   ii. F(A, B, C, D)= $\sum$m(1,3,4,5,10,11,12,13,14,15)
4. (a) Simplify the following boolean function F(A,B,C,D,E) = π(0,2,4,6,9,13,21,23,25,29,31). **[7M]**
   (b) Simplify the following boolean functions to a minimum number of literals. **[7M]**
   i. x+x'y
   ii. x(x'+y)
   iii. x'y'z+x'yz+xy'

UNIT – III

5. (a) Implement a full adder circuit using half adder circuits and OR gate. **[7M]**
   (b) Design a BCD to 2421 Code Converter Circuit. **[7M]**
6. Realize the following Boolean function using the following MUX **[14M]**
   F (A, B, C, D) = $\sum$m (1, 4, 5, 7, 9, 12, 13) using 16X1 MUX and 8X1 MUX

UNIT – IV

7. (a) Explain the characteristics of JK flip-flop with the help of logic diagram, characteristic table and characteristic equation. **[7M]**

   (b) Explain the design procedure for 3-bit binary counter using T-flip-floP. **[7M]**

8. (a) Design a BCD Ripple counter using JK Flip Flops. **[7M]**

   (b) Design a 4 bit Johnson counter with initial value to be 0000 using D Flip flops. **[7M]**

UNIT – V

9. (a) Using PROM, realize the following expressions **[7M]**
   F1 (a, b, c) = $\sum$m (0, 1, 3, 5, 7)
   F2 (a, b, c) = $\sum$m (1, 2, 5, 6)

   (b) Implement the circuit with a PLA **[7M]**
   F1 (a, b, c) = $\sum$m (0, 1, 3, 4)
   F2 (a, b, c) = $\sum$m (1, 2, 3, 4, 5)

10. Implement the following Boolean functions given in sum of min terms using PAL **[14M]**
    W(A, B, C, D) = $\sum$m (2,12,13)
    X(A,B, C, D) = $\sum$m (7,8,9,10,11,12,13,14,15)
    Y(A, B,C, D) = $\sum$m (0,2,3,4,5,6,7,8,9,10,11,15)
    Z(A, B, C, D) = $\sum$m (1,2,8,12,13)

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