Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC020

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Four Year B.Tech III Semester End Examinations (Supplementary) - July, 2018

Regulation: IARE – R16

DIGITAL LOGIC DESIGN

Time: 3 Hours **(Common to CSE | IT)** **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Perform the subtraction operation using 2's complement of the subtrahend **[7M]**
   i. $(5C)_{16}$ – $(3F)_{16}$
   ii. $(C0)_{16}$ – $(7A)_{16}$
   (b) Convert the following to the designated bases **[7M]**
   a. $(1000)_2$ to ( ) gray
   b. $(22.64)_{10}$ to ( )$_{16}$
   c. $(A72F)_{16}$ to ( )$_8$

2. (a) Write about binary logic in detail and explain binary addition and binary subtraction with examples. **[7M]**
   (b) Explain why Excess- 3 is self complementing code with an example. **[7M]**

UNIT – II

3. (a) Write the truth table for DeMorgans theorem by taking an example. **[7M]**
   (b) Simplify the boolean function F(w,x,y,z)=$\sum(1,3,7,11,15)$ that has the don't-care conditions d(w,x,y,z)=$\sum(0,2,5)$ **[7M]**

4. (a) Implement the following Boolean functions using the following logic **[7M]**
   i. (AB+CD) using NAND- NAND Realization
   ii. (A+B) (C+D) using NOR- NOR Realization
   (b) Simplify the following using four- variable K-map **[7M]**
   i. $w'z + xz + x'y + wx'z$
   ii. $B'D + A'BC' + AB'C + ABC'$

UNIT – III

5. (a) Explain the working of 2-bit magnitude comparator with the help truth table and logic diagram. **[7M]**

   (b) Enumerate the implementation of full-adder using two half-adders and an OR gate, for the following boolean expressions: **[7M]**

   $S = x'y'z + x'yz' + xy'z' + xyz$

   $C = xy + xz + yz$

6. (a) Show the construction of a 2-to-4-line decoder with an enable input constructed with NAND gates, construct the corresponding truth table for the same. **[7M]**

   (b) Implement the half adder using decoder and multiplexer for the following simplified boolean function **[7M]**

   $S = x'y + xy'$

   $C = xy$

UNIT – IV

7. (a) Explain the process of construction of a master-slave JK flip-flop using NAND gates. **[7M]**

   (b) Enumerate the construction of RS flip-flop with the help of logic diagram and characteristic table for the same. **[7M]**

8. (a) Explain the excitation table for the 3-bit binary counter and write the simplified maps for the excitation table based on flip-flop input function. **[7M]**

   (b) Construct the toggle flip-flop. Derive the characteristic table and characteristic equation. **[7M]**

UNIT – V

9. (a) Using PROM, realize the following expressions **[7M]**

   F1 (a, b, c) = $\sum$ (0, 1, 3, 5, 7)

   F2 (a, b, c) = $\sum$ (1, 2, 5, 6)

   (b) Implement the circuit with a PLA **[7M]**

   F1 (a, b, c) = $\sum$ (0, 1, 3, 4)

   F2 (a, b, c) = $\sum$ (1, 2, 3, 4, 5)

10. (a) Implement the Combinational circuit defined by the function with a PAL.

    f1(A, B, C, D) = $\sum$(0, 2, 5, 7, 8, 10, 12, 13) **[7M]**

    (b) Design a BCD to excess-3 code converter and implement using suitable PLA. **[7M]**