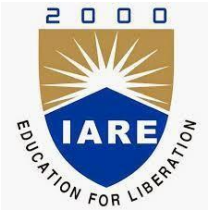
LECTURE NOTES ON

ANALOG ELECTRONICS

B.Tech III semester (IARE-R18)

Mrs.M.Sreevani
(Assistant professor)
Mr.P.Sandeep Kumar
(Assistant professor)



ELECRTONICS AND COMMUNICATION ENGINEERING
INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)
DUNDIGAL, HYDERABAD – 500043

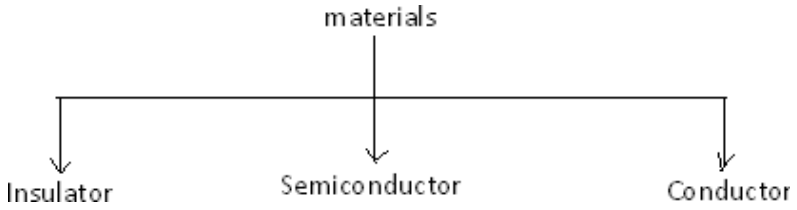
MODULE-I

DIODE CIRCUITS

P-N junction diode, I-V characteristics of a diode; review of half-wave and full-wave rectifiers, clamping and clipping circuits. Input output characteristics of BJT in CB, CE, CC configurations, biasing circuits, Load line analysis, common emitter, common base and common collector amplifiers; Small signal equivalent circuits.

INTRODUCTON

Based on the electrical conductivity all the materials in nature are classified as insulators, semiconductors, and conductors.

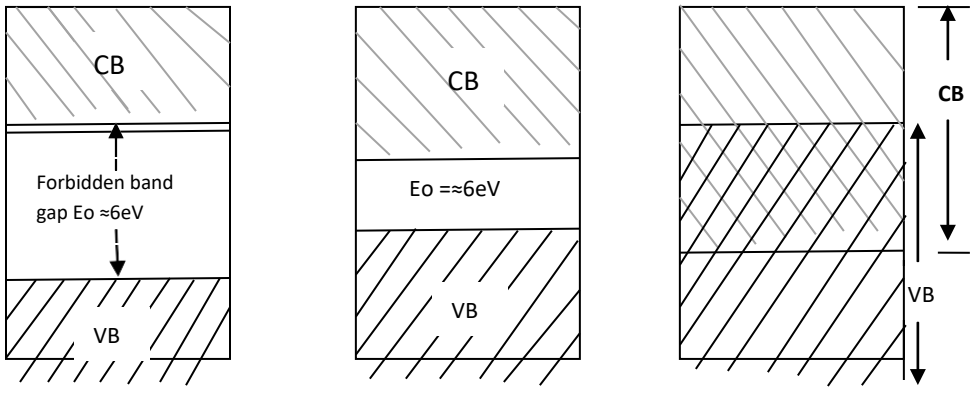


Insulator: An insulator is a material that offers a very low level (or negligible) of conductivity when voltage is applied. Eg: Paper, Mica, glass, quartz. Typical resistivity level of an insulator is of the order of 10^{10} to 10^{12} Ω-cm. The energy band structure of an insulator is shown in the fig.1.1. Band structure of a material defines the band of energy levels that an electron can occupy. Valance band is the range of electron energy where the electron remain bended too the atom and do not contribute to the electric current. Conduction bend is the range of electron energies higher than valance band where electrons are free to accelerate under the influence of external voltage source resulting in the flow of charge.

The energy band between the valance band and conduction band is called as forbidden band gap. It is the energy required by an electron to move from balance band to conduction band i.e. the energy required for a valance electron to become a free electron.

$$1 \text{ eV} = 1.6 \times 10^{-19} \text{ J}$$

For an insulator, as shown in the fig.1.1 there is a large forbidden band gap of greater than 5Ev. Because of this large gap there a very few electrons in the CB and hence the conductivity of insulator is poor. Even an increase in temperature or applied electric field is insufficient to transfer electrons from VB to CB.



Insulator Semiconductor Conductor

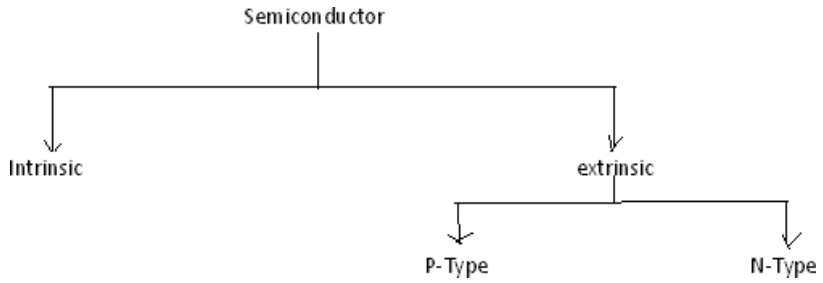
FiG:1.1 Energy band diagrams insulator, semiconductor and conductor

Conductors: A conductor is a material which supports a generous flow of charge when a voltage is applied across its terminals. i.e. it has very high conductivity. Eg: Copper, Aluminum, Silver, Gold. The resistivity of a conductor is in the order of 10^{-4} and 10^{-6} Ω-cm. The Valance and conduction bands overlap (fig1.1) and there is no energy gap for the electrons to move from valance band to conduction band. This implies that there are free electrons in CB even at absolute zero temperature (0K). Therefore at room temperature when electric field is applied large current flows through the conductor.

Semiconductor: A semiconductor is a material that has its conductivity somewhere between the insulator and conductor. The resistivity level is in the range of 10 and 10^4 Ω-cm. Two of the most commonly used are Silicon (Si=14 atomic no.) and germanium (Ge=32 atomic no.). Both have 4 valance electrons. The forbidden band gap is in the order of 1eV. For eg., the band gap energy for Si, Ge and GaAs is 1.21, 0.785 and 1.42 eV, respectively at absolute zero temperature (0K). At 0K and at low temperatures, the valance band electrons do not have sufficient energy to move from V to CB. Thus semiconductors act a insulators at 0K. as the temperature increases, a large number of valance electrons acquire sufficient energy to leave the VB, cross the forbidden bandgap and reach CB. These are now free electrons as they can move freely under the influence of electric field. At room temperature there are sufficient electrons in the CB and hence the semiconductor is capable of conducting some current at room temperature.

Inversely related to the conductivity of a material is its resistance to the flow of charge or current. Typical resistivity values for various materials' are given as follows.

Semiconductor Types



A pure form of semiconductors is called as intrinsic semiconductor. Conduction in intrinsic sc is either due to thermal excitation or crystal defects. Si and Ge are the two most important semiconductors used. Other examples include Gallium arsenide GaAs, Indium Antimonide (InSb) etc.

Let us consider the structure of Si. A Si atomic no. is 14 and it has 4 valance electrons. These 4 electrons are shared by four neighboring atoms in the crystal structure by means of covalent bond. Fig. 1.2a shows the crystal structure of Si at absolute zero temperature (0K). Hence a pure SC acts has poor conductivity (due to lack of free electrons) at low or absolute zero temperature.

The absence of electrons in covalent bond is represented by a small circle usually referred to as hole which is of positive charge. Even a hole serves as carrier of electricity in a manner similar to that of free electron. In a pure semiconductor, the number of holes is equal to the number of free electrons.

EXTRINSIC SEMICONDUCTOR

Intrinsic semiconductor has very limited applications as they conduct very small amounts of current at room temperature. The current conduction capability of intrinsic semiconductor can be increased significantly by adding a small amounts impurity to the intrinsic semiconductor. By adding impurities it becomes impure or extrinsic semiconductor. This process of adding impurities is called as doping. The amount of impurity added is 1 part in 10^6 atoms.

N type semiconductor: If the added impurity is a pentavalent atom then the resultant semiconductor is called N-type semiconductor. Examples of pentavalent impurities are Phosphorus, Arsenic, Bismuth, Antimony etc.

P type semiconductor: If the added impurity is a trivalent atom then the resultant semiconductor is called P-type semiconductor. Examples of trivalent impurities are Boron, Gallium , indium etc. Thus in P type sc , holes are majority carriers and electrons are minority carriers. Since each trivalent impurity atoms are capable accepting an electron, these are called as acceptor atoms. The following fig 1.5b shows the pictorial representation of P type sc

- The conductivity of N type sc is greater than that of P type sc as the mobility of electron is greater than that of hole.
- For the same level of doping in N type sc and P type sc, the conductivity of an N type sc is around twice that of a P type sc.

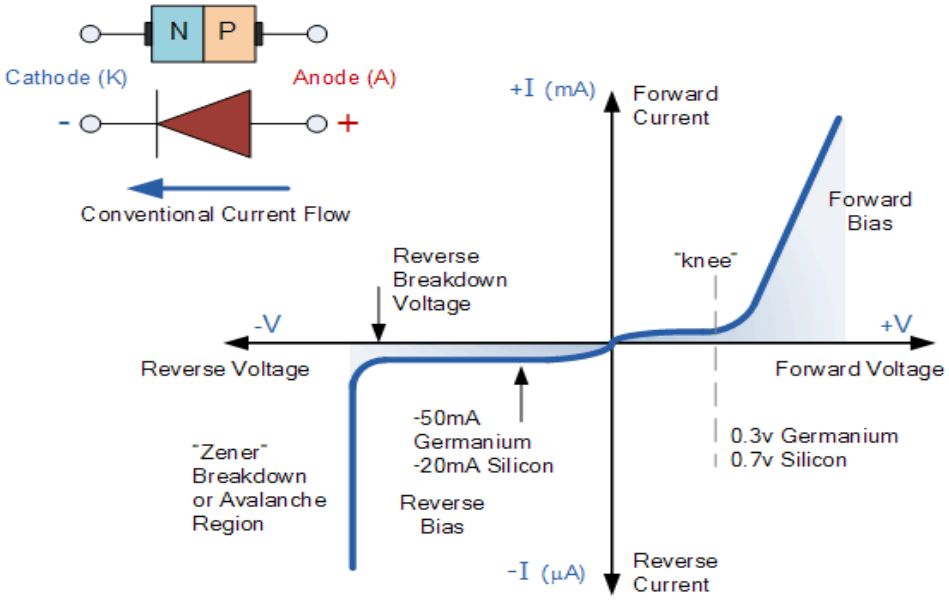
A *PN Junction Diode* is one of the simplest semiconductor devices around, and which has the characteristic of passing current in only one direction only. However, unlike a resistor, a diode does not behave linearly with respect to the applied voltage as the diode has an exponential current-voltage (I-V) relationship and therefore we cannot described its operation by simply using an equation such as Ohm's law.

If a suitable positive voltage (forward bias) is applied between the two ends of the PN junction, it can supply free electrons and holes with the extra energy they require to cross the junction as the width of the depletion layer around the PN junction is decreased.

By applying a negative voltage (reverse bias) results in the free charges being pulled away from the junction resulting in the depletion layer width being increased. This has the effect of increasing or decreasing the effective resistance of the junction itself allowing or blocking current flow through the diode.

Then the depletion layer widens with an increase in the application of a reverse voltage and narrows with an increase in the application of a forward voltage. This is due to the differences in the electrical properties on the two sides of the PN junction resulting in physical changes taking place. One of the results produces rectification as seen in the PN junction diodes static I-V (current-voltage) characteristics. Rectification is shown by an asymmetrical current flow when the polarity of bias voltage is altered as shown below.

Junction Diode Symbol and Static I-V Characteristics



But before we can use the PN junction as a practical device or as a rectifying device we need to firstly bias the junction, ie connect a voltage potential across it. On the voltage axis above, "Reverse Bias" refers to an external voltage potential which increases the potential barrier. An external voltage which decreases the potential barrier is said to act in the "Forward Bias" direction.

There are two operating regions and three possible "biasing" conditions for the standard **Junction Diode** and these are:

1. Zero Bias – No external voltage potential is applied to the PN junction diode.

2. Reverse Bias – The voltage potential is connected negative, (-ve) to the P-type material and positive, (+ve) to the N-type material across the diode which has the effect of Increasing the PN junction diode's width.

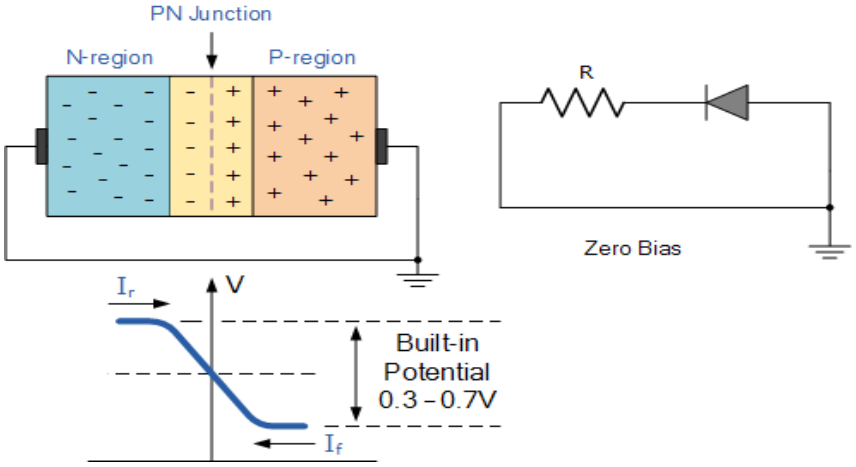
3. Forward Bias – The voltage potential is connected positive, (+ve) to the P-type material and negative, (-ve) to the N-type material across the diode which has the effect of Decreasing the PN junction diodes width.

Zero Biased Junction Diode

When a diode is connected in a Zero Bias condition, no external potential energy is applied to the PN junction. However if the diodes terminals are shorted together, a few holes (majority carriers) in the P-type material with enough energy to overcome the potential barrier will move across the junction against this barrier potential. This is known as the "Forward Current" and is referenced as IF

Likewise, holes generated in the N-type material (minority carriers), find this situation favourable and move across the junction in the opposite direction. This is known as the "Reverse Current" and is referenced as IR. This transfer of electrons and holes back and forth across the PN junction is known as diffusion, as shown below.

Zero Biased PN Junction Diode



The potential barrier that now exists discourages the diffusion of any more majority carriers across the junction. However, the potential barrier helps minority carriers (few free electrons in the P-region and few holes in the N-region) to drift across the junction.

The minority carriers are constantly generated due to thermal energy so this state of equilibrium can be broken by raising the temperature of the PN junction causing an increase in the generation of minority carriers, thereby resulting in an increase in leakage current but an electric current cannot flow since no circuit has been connected to the PN junction.

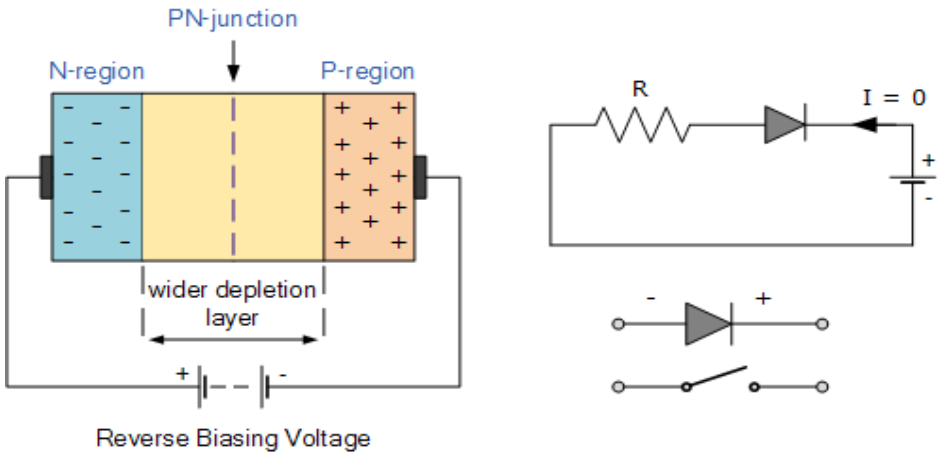
Reverse Biased PN Junction Diode

When a diode is connected in a Reverse Bias condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material.

The positive voltage applied to the N-type material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode.

The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.

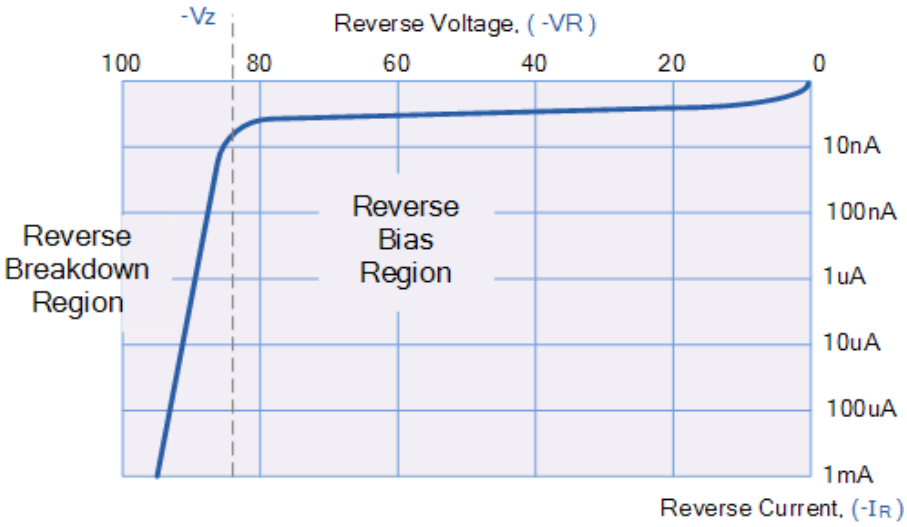
Increase in the Depletion Layer due to Reverse Bias



This condition represents a high resistance value to the PN junction and practically zero current flows through the junction diode with an increase in bias voltage. However, a very small leakage current does flow through the junction which can be measured in micro-amperes, (μA).

One final point, if the reverse bias voltage Vr applied to the diode is increased to a sufficiently high enough value, it will cause the diode's PN junction to overheat and fail due to the avalanche effect around the junction. This may cause the diode to become shorted and will result in the flow of maximum circuit current, and this shown as a step downward slope in the reverse static characteristics curve below.

Reverse Characteristics Curve for a Junction Diode



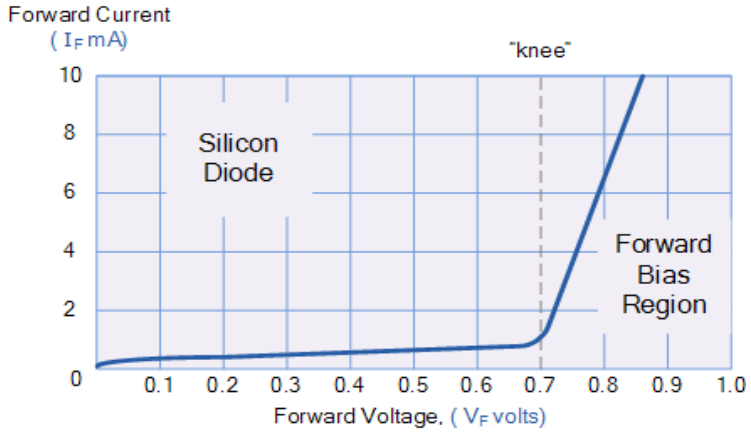
Sometimes this avalanche effect has practical applications in voltage stabilizing circuits where a series limiting resistor is used with the diode to limit this reverse breakdown current to a preset maximum value thereby producing a fixed voltage output across the diode. These types of diodes are commonly known as Zener Diodes and are discussed in a later tutorial.

Forward Biased PN Junction Diode

When a diode is connected in a Forward Bias condition, a negative voltage is applied to the N-type material and a positive voltage is applied to the P-type material. If this external voltage becomes greater than the value of the potential barrier, approx. 0.7 volts for silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow.

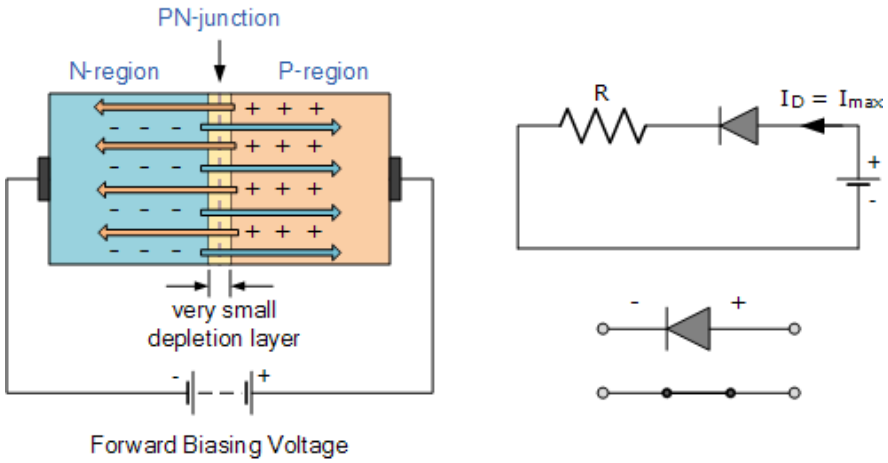
This is because the negative voltage pushes or repels electrons towards the junction giving them the energy to cross over and combine with the holes being pushed in the opposite direction towards the junction by the positive voltage. This results in a characteristics curve of zero current flowing up to this voltage point, called the "knee" on the static curves and then a high current flow through the diode with little increase in the external voltage as shown below.

Forward Characteristics Curve for a Junction Diode



The application of a forward biasing voltage on the junction diode results in the depletion layer becoming very thin and narrow which represents a low impedance path through the junction thereby allowing high currents to flow. The point at which this sudden increase in current takes place is represented on the static I-V characteristics curve above as the "knee" point.

Reduction in the Depletion Layer due to Forward Bias



This condition represents the low resistance path through the PN junction allowing very large currents to flow through the diode with only a small increase in bias voltage. The actual potential difference across the junction or diode is kept constant by the action of the depletion layer at approximately 0.3v for germanium and approximately 0.7v for silicon junction diodes.

Since the diode can conduct "infinite" current above this knee point as it effectively becomes a short circuit, therefore resistors are used in series with the diode to limit its current flow. Exceeding its maximum forward current specification causes the device to dissipate more power in the form of heat than it was designed for resulting in a very quick failure of the device.

Junction Diode Summary

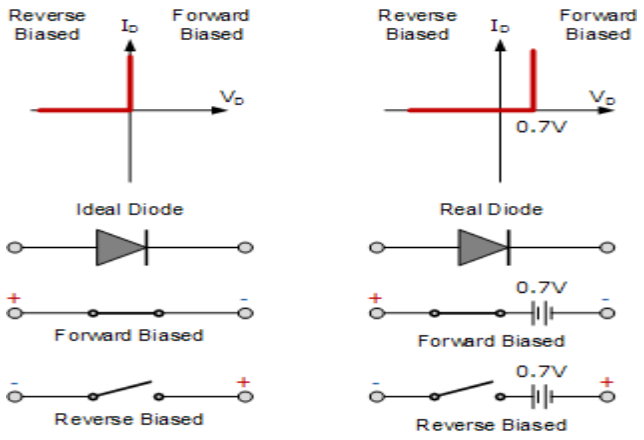
- The PN junction region of a **Junction Diode** has the following important characteristics:
- Semiconductors contain two types of mobile charge carriers, "Holes" and "Electrons".
- The holes are positively charged while the electrons negatively charged.
- A semiconductor may be doped with donor impurities such as Antimony (N-type doping), so that it contains mobile charges which are primarily electrons.
- A semiconductor may be doped with acceptor impurities such as Boron (P-type doping),

so that it contains mobile charges which are mainly holes.

- The junction region itself has no charge carriers and is known as the depletion region.
- The junction (depletion) region has a physical thickness that varies with the applied voltage.
- When a diode is Zero Biased no external energy source is applied and a natural Potential Barrier is developed across a depletion layer which is approximately 0.5 to 0.7v for silicon diodes and approximately 0.3 of a volt for germanium diodes.
- When a junction diode is Forward Biased the thickness of the depletion region reduces and the diode acts like a short circuit allowing full current to flow.
- When a junction diode is Reverse Biased the thickness of the depletion region increases and the diode acts like an open circuit blocking any current flow, (only a very small leakage current).

We have also seen above that the diode is two terminal non-linear device whose I-V characteristic are polarity dependent as depending upon the polarity of the applied voltage, VD the diode is either *Forward Biased*, VD > 0 or *Reverse Biased*, VD < 0. Either way we can model these current-voltage characteristics for both an ideal diode and for a real silicon diode as shown:

Junction Diode Ideal and Real Characteristics



RECTIFIERS:

INTRODUCTION

For the operation of most of the electronics devices and circuits, a d.c. source is required. So it is advantageous to convert domestic a.c. supply into d.c voltages. The process of converting a.c. voltage into d.c. voltage is called as rectification. This is achieved with i) Step-down Transformer, ii) Rectifier, iii) Filter and iv) Voltage regulator circuits.

These elements constitute d.c. regulated power supply shown in the fig 1 below.

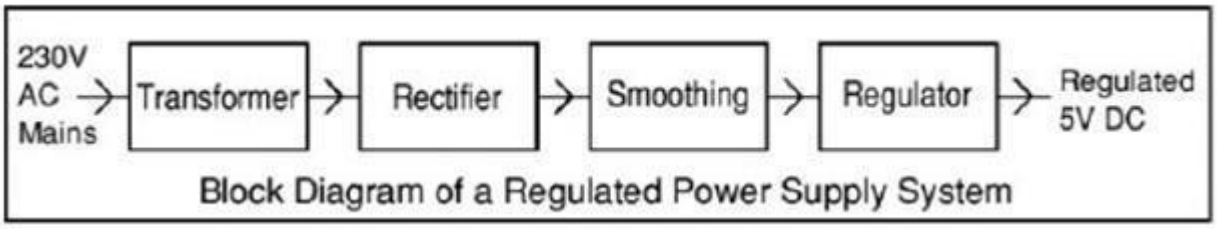


Fig 2.1: Block Diagram of regulated D.C Power Supply

- ✓ Transformer – steps down 230V AC mains to low voltage AC.
- ✓ Rectifier – converts AC to DC, but the DC output is varying.
- ✓ Smoothing – smooth the DC from varying greatly to a small ripple.
- ✓ Regulator – eliminates ripple by setting DC output to a fixed voltage.

The block diagram of a regulated D.C. power supply consists of step-down transformer, rectifier, filter, voltage regulator and load. An ideal regulated power supply is an electronics circuit designed to provide a predetermined d.c. voltage Vo which is independent of the load current and variations in the input voltage ad temperature. If the output of a regulator circuit is a AC voltage then it is termed as voltage stabilizer, whereas if the output is a DC voltage then it is termed as voltage regulator.

RECTIFIER

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional Waveform, with a non-zero average component. A rectifier is a device, which converts a.c. voltage (bi-directional) to pulsating d.c. voltage (Unidirectional).

Characteristics of a Rectifier Circuit:

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional waveform, with a non-zero average component.

A rectifier is a device, which converts a.c. voltage (bi-directional) to pulsating d.c..Load currents: They are two types of output current. They are average or d.c. current and RMS currents.

Average or DC current: The average current of a periodic function is defined as the area of one cycle of the curve divided by the base.

i) Effective (or) R.M.S current:

The effective (or) R.M.S. current squared ofa periodic function of time is given by the area of one cycle of the curve, which represents the square of the function divided by the base.

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d(wt)}$$

ii) Peak factor:

It is the ratio of peak value to Rms value

$$\text{Peak factor} = \frac{peakvalue}{rmsvalue}$$

iii) Form factor:

It is the ratio of Rms value to average value

$$\text{Form factor} = \frac{Rmsvalue}{averagevalue}$$

iv) Ripple Factor:

It is defined as ration of R.M.S. value of a.c. component to the d.c. component in the output is known as “Ripple Factor”.

v) Efficiency :

It is the ratio of d.c output power to the a.c. input power. It signifies, how efficiently the rectifier circuit converts a.c. power into d.c. power.

$$\eta = \frac{o/p\ power}{i/p\ power}$$

vi) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction.

vii) Transformer Utilization Factor (UTF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the Transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{p_{ac(rated)}}$$

viii) % Regulation:

The variation of the d.c. output voltage as a function of d.c. load current is called regulation. The percentage regulation is defined as

$$\%\ \text{Re}\ gulation = \frac{V_{NL} - V_{FL}}{V_{FL}} * 100$$

For an ideal power supply, % Regulation is zero.

CLASSIFICATION OF RECTIFIERS

Using one or more diodes in the circuit, following rectifier circuits can be designed.

1) Half - Wave Rectifier
2) Full – Wave Rectifier
3) Bridge Rectifier

HALF-WAVE RECTIFIER:

A Half – wave rectifier as shown in **fig 1.2** is one, which converts a.c. voltage into a pulsating voltage using only one half cycle of the applied a.c. voltage.

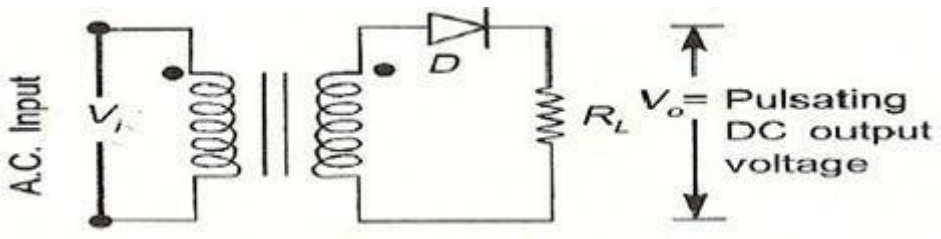


Fig 1.2: Basic structure of Half-Wave Rectifier

The a.c. voltage is applied to the rectifier circuit using step-down transformer-rectifying element i.e., p-n junction diode and the source of a.c. voltage, all connected is series. The a.c. voltage is applied to the rectifier circuit using step-down transformer

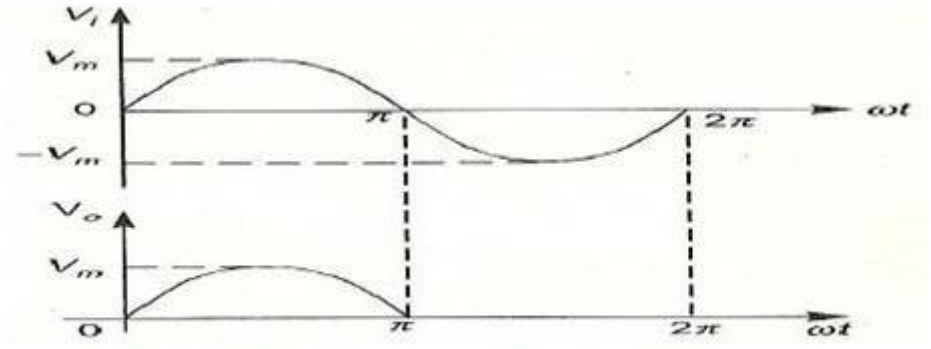


fig 3 Input and output waveforms of a Half wave rectifier

$V=V_m \sin(wt)$

The input to the rectifier circuit, Where V_m is the peak value of secondary a.c. voltage.

Operation:

For the positive half-cycle of input a.c. voltage, the diode D is forward biased and hence it conducts. Now a current flows in the circuit and there is a voltage drop across RL.

For the negative half-cycle of input, the diode D is reverse biased and hence it does not Conduct. Now no current flows in the circuit i.e., i=0 and Vo=0. Thus for the negative half- cycle no power is delivered to the load.

Let a sinusoidal voltage Vi be applied to the input of the rectifier.

Then $V=V_m \sin(wt)$ Where V_m is the maximum value of the secondary voltage. Let the diode be idealized to piece-wise linear approximation with resistance Rf in the forward direction i.e., in the ON state and Rr (=∞) in the reverse direction i.e., in the OFF state. Now the current 'i' in the diode (or) in the load resistance RL is given by $V=V_m \sin(wt)$

DISADVANTAGES OF HALF-WAVE RECTIFIER:

1. The ripple factor is high.
2. The efficiency is low.
3. The Transformer Utilization factor is low.

FULL WAVE RECTIFIER:

A full-wave rectifier converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. In order to rectify both the half cycles of ac input, two diodes are used in this circuit. The diodes feed a common load RL with the help of a center-tap transformer. A center-tap transformer is the one, which produces two sinusoidal waveforms of same magnitude and frequency but out of phase with respect to the ground in the secondary winding of the transformer.

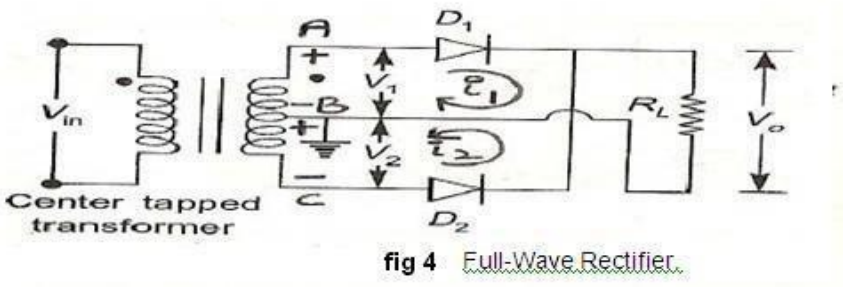


fig 4 Full-Wave Rectifier

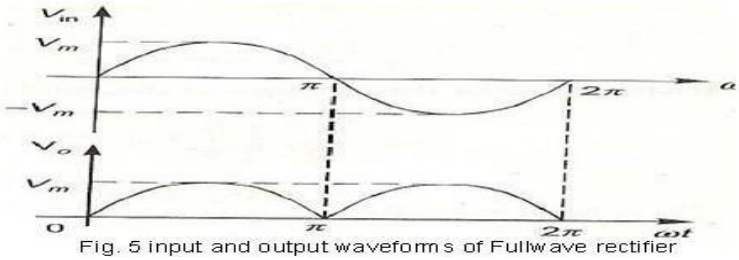


Fig. 5 input and output waveforms of Fullwave rectifier

Fig. 5 shows the input and output wave forms of the ckt.

During positive half of the input signal, anode of diode D1 becomes positive and at the same time the anode of diode D2 becomes negative. Hence D1 conducts and D2 does not conduct. The load current flows through D1 and the voltage drop across RL will be equal to the input voltage.

During the negative half cycle of the input, the anode of D1 becomes negative and the anode of D2 becomes positive. Hence, D1 does not conduct and D2 conducts. The load current flows through D2 and the voltage drop across RL will be equal to the input voltage. It is noted that the load current flows in the both the half cycles of ac voltage and in the same direction through the load resistance.

i) AVERAGEVOLTAGE

$$V_{dc} = I_{dc}.R_L = \frac{2I_m}{\pi}.R_L \quad \text{We know } I_m = \frac{V_m}{R_S + R_f + R_L}$$

$$\therefore V_{dc} = \frac{2.V_m.R_L}{\pi(R_S + R_f + R_L}$$

$$If\,(R_s + R_f) << R_L$$

$$V_{dc} = \frac{2V_m}{\pi} = 0.637V_m.$$

ii) AVERAGE CURRENT

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} id\theta = \frac{1}{2\pi}\int_0^{2\pi} I_m \sin\theta d\theta$$

$$= \frac{I_m}{2\pi}\left[\int_0^{\pi} \sin\theta d\theta - \int_{\pi}^{2\pi} \sin\theta d\theta\right]$$

$$= \frac{I_m}{2\pi}[(-2)(-2)]$$

$$= \frac{I_m}{2\pi}.4 = \frac{2I_m}{\pi} = 0.637 I_m .$$

$$\boxed{I_{dc} = 0.637 I_m.}$$

$$\therefore I_{DC}\ FWR = 2\ I_{DC}\ HWR.$$

iii) RMS VOLTAGE:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d(wt)}$$

$$V_{rms} = \sqrt{\frac{1}{2\Pi}\int_0^{2\Pi} (V_m sim(wt))^2 d(wt)}$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

IV) RMS CURRENT

$$\boxed{I_{rms} = \frac{2I_m}{\Pi}}$$

vi) FORM FACTOR

$$\text{Form factor} = \frac{Rms\ value}{averagevalue}$$

$$\text{Form factor} = \frac{(V_m/\sqrt{2})}{2V_m/\Pi}$$

Form Factor =1.11

vii) Ripple Factor:

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

for FWR,

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad \& \quad I_{DC} = \frac{2I_m}{\pi}$$

$$\therefore \gamma_{FWR} = \sqrt{\left(\frac{I_m}{\sqrt{2}} / \frac{2I_m}{\pi}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{3.1416}{2 \times 1.414}\right)^2 - 1} = 0.483$$

V) Efficiency:

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100\%$$

For FWR, $P_{dc} = I_{dc}^2 . R_L = \left(\frac{2}{\pi} . I_m\right)^2 . R_L$

$P_{ac} = I^2_{rms} (R_f + R_S + R_L)$

$$\left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_S + R_L)$$

$$\eta = \frac{\frac{I^2_m 4}{\pi^2} . R_L}{\frac{I^2 m^2}{2} . (R_f + R_s + R_L)}$$

$$If (R_f + R_S) << R_L$$

$$\eta = \frac{4}{\pi^2} . \frac{2}{1} = \frac{8}{\pi^2} = 0.812 = 81.2\%$$

viii) Transformer Utilization Factor (TUF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

a) $\text{TUF (Secondary)} = \dfrac{P_{dc} \text{ delivered to load}}{\text{AC power rating of transformer secondary}}$

b) Since both the windings are used $\text{TUF}_{FWR} = 2\ \text{TUF}_{HWR}$

$= \quad 2 \times 0.287 = 0.574$

c) TUF primary = Rated efficiency $= \frac{P_{dc}}{P_{ac}} \times 100 = 81.2\%$

d) Average $= \frac{0.812 + 0.574}{2} = 0.693$

ix) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half- cycle. For half- wave rectifier, PIV is 2Vm.

x) % Regulation

$$\text{Voltage regulation} = \frac{I_{dc}(R_s + R_f)}{\frac{2V_m}{\pi} - I_{DC}(R_f + R_S)}$$

Advantages:

1) Ripple factor = 0.482 (against 1.21 for HWR)
2) Rectification efficiency is 0.812 (against 0.405 for HWR)
3) Better TUF (secondary) is 0.574 (0.287 for HWR)
4) No core saturation problem

Disadvantages:

1) Requires center tapped transformer.

BIPOLAR JUNCTION TRANSISTOR

INTRODUCTION

A bipolar junction transistor (BJT) is a three terminal device in which operation depends on the interaction of both majority and minority carriers and hence the name bipolar. The BJT is analogues to vacuum triode and is comparatively smaller in size. It is used as amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites and other modern communication systems.

CONSTRUCTION OF BJT AND ITS SYMBOLS

The **Bipolar Transistor** basic construction consists of two PN-junctions producing three connecting terminals with each terminal being given a name to identify it from the other two. These three terminals are known and labelled as the Emitter (E), the Base (B) and the Collector (C) respectively. There are two basic types of bipolar transistor construction, PNP and NPN, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made.

Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage. The transistor's ability to change between these two states enables it to have two basic functions: "switching" (digital electronics) or "amplification" (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

1. Active Region - the transistor operates as an amplifier and Ic = β.Ib
2. Saturation - the transistor is "fully-ON" operating as a switch and Ic = I(saturation)
3. Cut-off - the transistor is "fully-OFF" operating as a switch and Ic = 0

Bipolar Transistors are current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing voltage applied to their base terminal acting like a current-controlled switch. The principle of operation of the two transistor types PNP and NPN, is exactly the same the only difference being in their biasing and the polarity of the power supply for each type.

Bipolar Transistor Construction

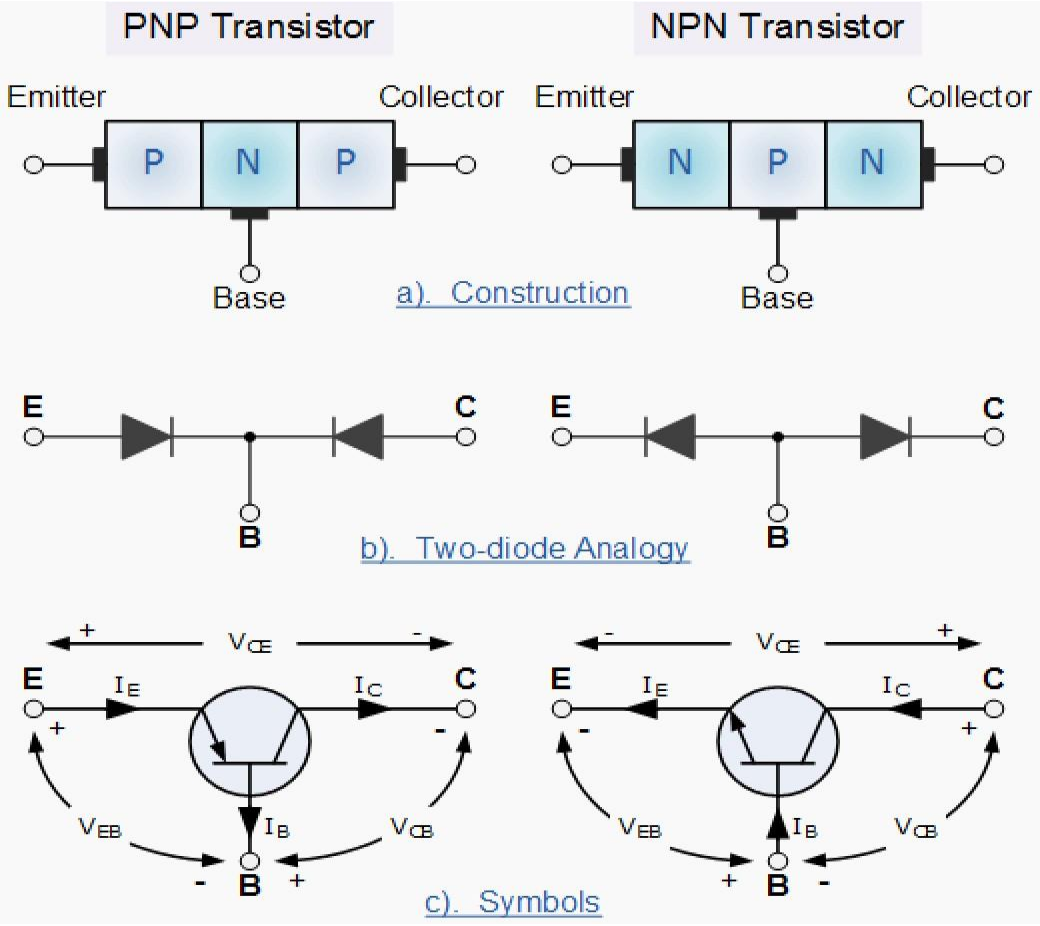


Fig 3.1 Bipolar Junction Transistor Symbol

The construction and circuit symbols for both the PNP and NPN bipolar transistor are given above with the arrow in the circuit symbol always showing the direction of "conventional current flow" between the base terminal and its emitter terminal. The direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

TRANSISTOR CURRENT COMPONENTS:

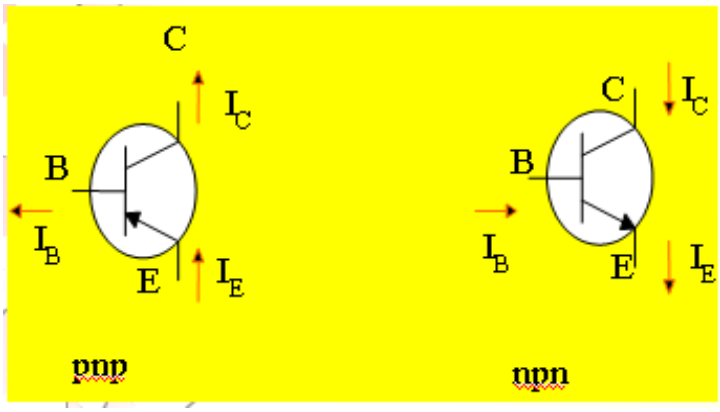


Fig 3.2 Bipolar Junction Transistor Current Components

The above fig 3.2 shows the various current components, which flow across the forward biased emitter junction and reverse- biased collector junction. The emitter current I_E consists of hole current I_{PE} (holes crossing from emitter into base) and electron current I_{nE} (electrons crossing from base into emitter).The ratio of hole to electron currents, I_{pE} / I_{nE} , crossing the emitter junction is proportional to the ratio of the conductivity of the p material to that of the n material. In a transistor, the doping of that of the emitter is made much larger than the doping of the base. This feature ensures (in p-n-p transistor) that the emitter current consists an almost entirely of holes. Such a situation is desired since the current which results from electrons crossing the emitter junction from base to emitter do not contribute carriers, which can reach the collector.

For a p-n-p transistor, I_{CO} consists of holes moving across J_C from left to right (base to collector) and electrons crossing J_C in opposite direction. Assumed referenced direction for I_{CO} i.e. from right to left, then for a p-n-p transistor, I_{CO} is negative. For an n-p-n transistor, I_{CO} is positive.The basic operation will be described using the pnp transistor. The operation of the pnp transistor is exactly the same if the roles played by the electron and hole are interchanged. One p-n junction of a transistor is reverse-biased, whereas the other is forward-biased.

Bipolar Transistor Configurations

As the **Bipolar Transistor** is a three terminal device, there are basically three possible ways to connect it within an electronic circuit with one terminal being common to both the input and output. Each method of connection responding differently to its input signal within a circuit as the static characteristics of the transistor vary with each circuit arrangement.

- 1. Common Base Configuration - has Voltage Gain but no Current Gain.
- 2 Common Emitter Configuration - has both Current and Voltage Gain.
- 3. Common Collector Configuration - has Current Gain but no Voltage Gain.

COMMON-BASE CONFIGURATION

Common-base terminology is derived from the fact that the : base is common to both input and output of t configuration. base is usually the terminal closest to or at ground potential. Majority carriers can cross the reverse-biased junction because the injected majority carriers will appear as minority carriers in the n-type material. All current directions will refer to conventional (hole) flow and the arrows in all electronic symbols have a direction defined by this convention.

Note that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch.

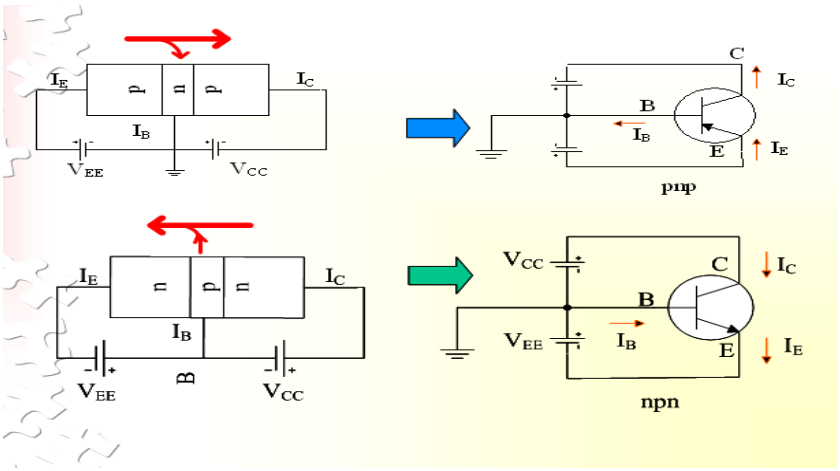


Fig 3.4 CB Configuration

To describe the behavior of common-base amplifiers requires two set of characteristics:

1. Input or driving point characteristics.
2. Output or collector characteristics

The output characteristics has 3 basic regions:

- Active region –defined by the biasing arrangements
- Cutoff region – region where the collector current is 0A
- Saturation region- region of the characteristics to the left of $V_{CB} = 0V$

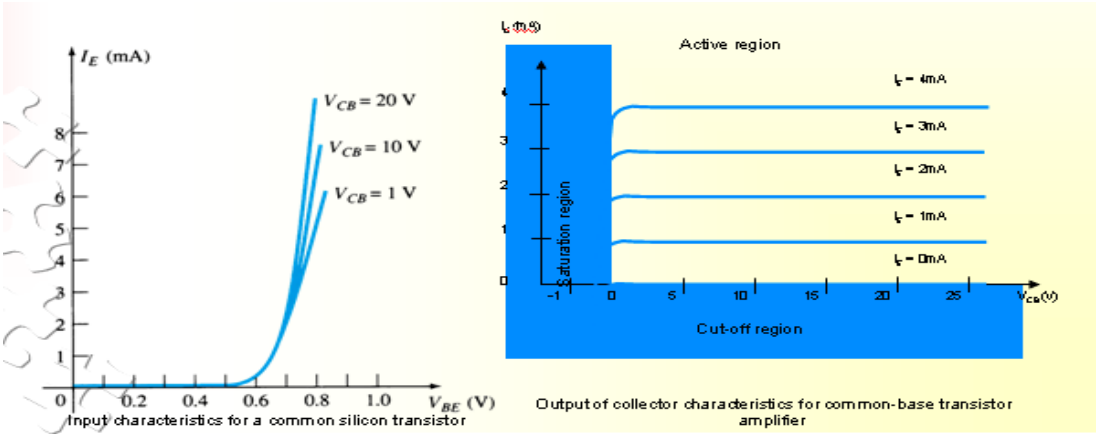


Fig 3.5 CB Input-Output Characteristics

Active region	Saturation region	Cut-off region
•IE increased, Ic increased •BE junction forward bias and CB junction reverse bias •Refer to the graf, Ic ≈ IE •Ic not depends on VCB •Suitable region for the transistor working as amplifier	• BE and CB junction is forward bias • Small changes in VCB will cause big different to Ic • The allocation for this region is to the left of VCB= 0 V.	• Region below the line of IE=0 A • BE and CB is reverse bias • no current flow at collector, only leakage current

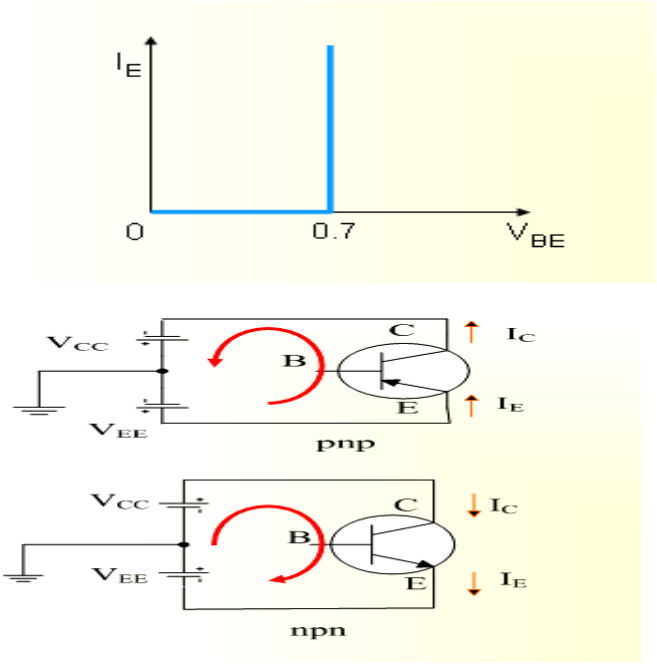


Fig 3.6 CE Configuration

TRANSISTOR AS AN AMPLIFIER

Common-Emitter Configuration

It is called common-emitter configuration since : emitter is common or reference to both input and output terminals. Emitter is usually the terminal closest to or at ground potential. Almost amplifier design is using connection of CE due to the high gain for current and voltage. Two set of characteristics are necessary to describe the behavior for CE ;input (base terminal) and output (collector terminal) parameters. Proper Biasing common-emitter configuration in active region.

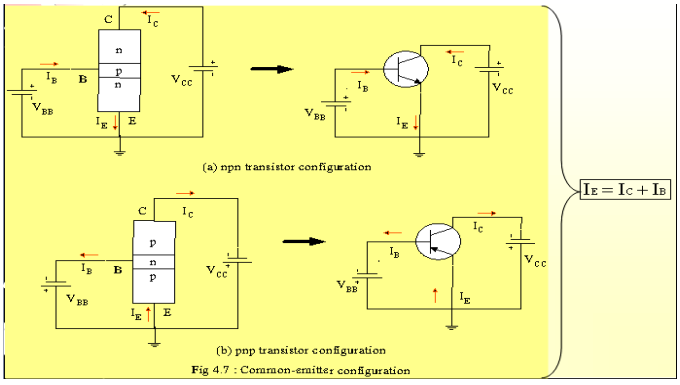


Fig 4.7 : Common-emitter configuration

Fig 3.8 CE Configuration

Base-emitter junction is forward bias Increasing V_{CE} will reduce I_B for different values.

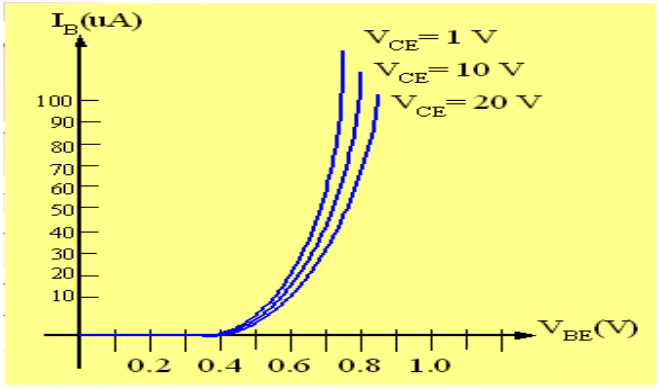


Fig 3.9a Input characteristics for common-emitter npn transistor

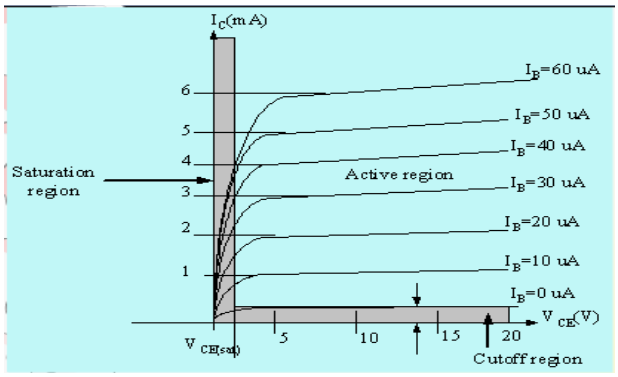
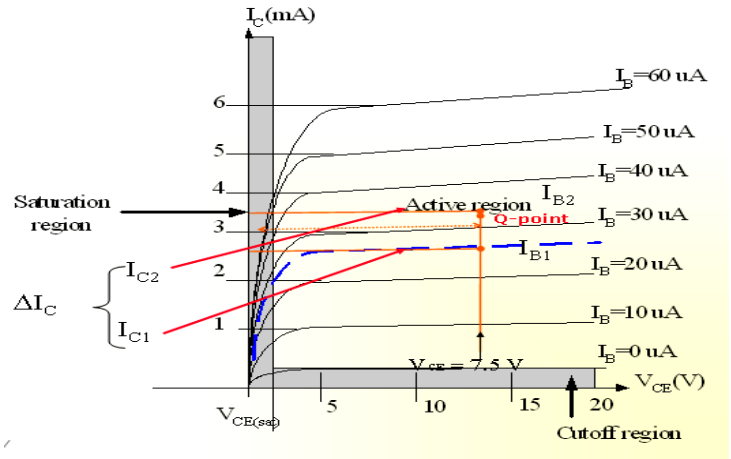


Fig 3.9b Output characteristics for common-emitter npn transistor



Relationship analysis between α and β

CASE 1

$I_E = I_C + I_B$ (1)

subtitute equ. $I_C = \beta I_B$ into (1) we get

$$I_E = (\beta + 1) I_B$$

CASE 2

known : $\alpha = \frac{I_C}{I_E} \Rightarrow I_E = \frac{I_C}{\alpha}$ (2)

known : $\beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta}$ (3)

subtitute (2) and (3) into (1) we get,

$$\alpha = \frac{\beta}{\beta + 1} \quad \text{and} \quad \beta = \frac{\alpha}{1 - \alpha}$$

COMMON – COLLECTOR CONFIGURATION

Also called emitter-follower(EF). It is called common-emitter configuration since both the signal source and the load share the collector terminal as a common connection point. The output voltage is obtained at emitter terminal. The input characteristic of common-collector configuration is similar with common-emitter configuration. Common-collector circuit configuration is provided with the load resistor connected from emitter to ground. It is used primarily for impedance- matching purpose since it has high input impedance and low output impedance.

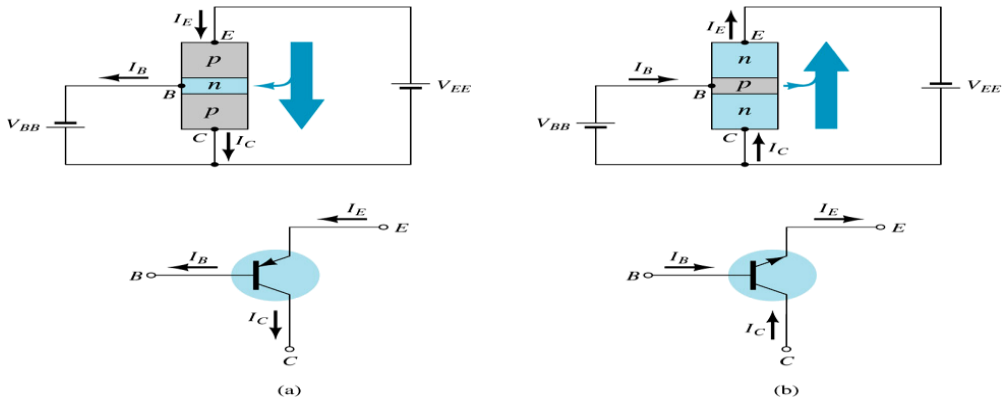


Fig 3.10 CC Configuration

For the common-collector configuration, the output characteristics are a plot of I_E vs V_{CE} for a range of values of I_B.

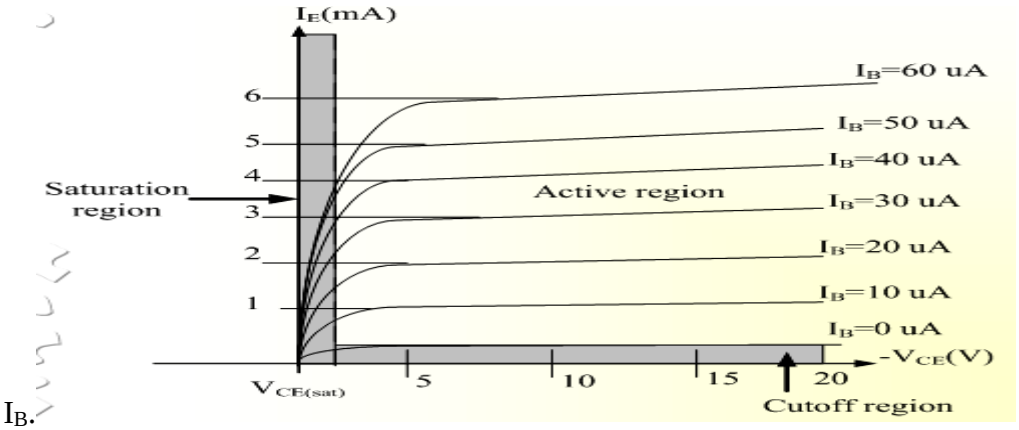


Fig 3.11 Output Characteristics of CC Configuration for npn Transistor

Limits of operation

Many BJT transistor used as an amplifier. Thus it is important to notice the limits of operations. At least 3 maximum values is mentioned in data sheet.

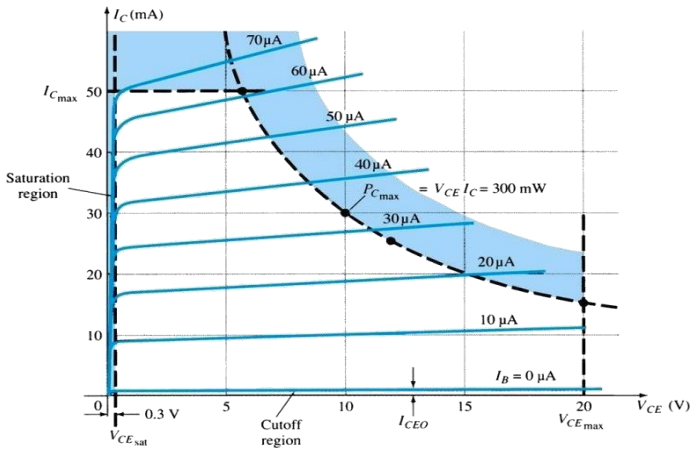
There are:

a) Maximum power dissipation at collector: P_{Cmax} or P_D

b) Maximum collector-emitter voltage: V_{CEmax} sometimes named as $V_{BR(CEO)}$ or V_{CEO}.

c) Maximum collector current: ICmax

There are few rules that need to be followed for BJT transistor used as an amplifier. The rules are: transistor need to be operate in active region! $I_C < I_{Cmax}$ $P_C < P_{Cmax}$



Note: V_{CE} is at maximum and I_C is at minimum (I_{CMAX}=I_{CEO}) in the cutoff region. I_C is at maximum and V_{CE} is at minimum (V_{CE} max = V_{cesat} = V_{CEO}) in the saturation region. The transistor operates in the active region between saturation and cutoff.

BJT HYBRID MODEL

Small signal low frequency transistor Models:
All the transistor amplifiers are two port networks having two voltages and two currents. The positive directions of voltages and currents are shown in **fig. 1**.

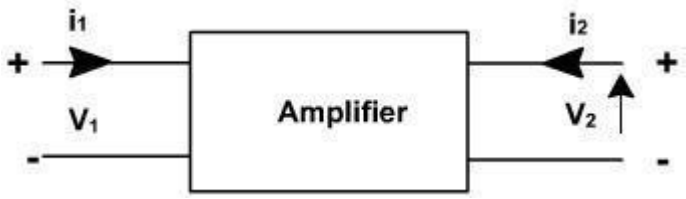


Fig. 1

A two-port network is represented by four external variables: voltage V_1 and current I_1 at the input port, and voltage V_2 and current I_2 at the output port, so that the two-port network can be treated as a black box modeled by the relationships between the four variables, V_1,V_2, I_1,I_2 . Out of four variables two can be selected as are independent variables and two are dependent variables. The dependent variables can be expressed interns of independent variables. This leads to various two port parameters out of which the following three are important:

1. Impedance parameters (z-parameters)
2. Admittance parameters (y-parameters)
3. Hybrid parameters (h-parameters)

Z-parameters

A two-port network can be described by z-parameters as

$V_2 = Z_{21}I_1 + Z_{22}I_2$

$V_1 = Z_{11}I_1 + Z_{12}I_2$

In matrix form, the above equation can be rewritten as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

Where

Input impedance with output port open circuited

$$z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0}$$

Reverse transfer impedance with input port open circuited

$$z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0}$$

Forward transfer impedance with output port open circuited

$$z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0}$$

Output impedance with input port open circuited

Y-parameters

A two-port network can be described by Y-parameters as

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$
$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

In matrix form, the above equation can be rewritten as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0}$$

Input admittance with output port short circuited

$$y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0}$$

Reverse transfer admittance with input port short circuited

$$y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0}$$

Forward transfer admittance with output port short circuited

$$y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0}$$

Output admittance with input port short circuited

Hybrid parameters (h-parameters)

If the input current I1 and output voltage V2 are taken as independent variables, the dependent variables V1 and I2 can be written as

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

Where h_{11}, h_{12}, h_{21}, h_{22} are called as hybrid parameters.

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0}$$

Input impedance with o/p port short circuited

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0}$$

Reverse voltage transfer ratio with i/p port open circuited

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0}$$

Forward voltage transfer ratio with o/p port short circuited

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$$

output impedance with i/p port open circuited

THE HYBRID MODEL FOR TWO PORT

NETWORK:

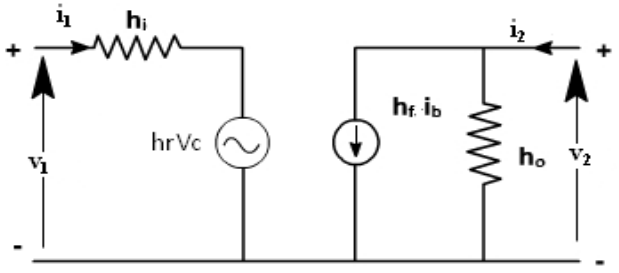
Based on the definition of hybrid parameters the mathematical model for two pert networks known as h-parameter model can be developed. The hybrid equations can be written as:

$$V_1 = h_i I_1 + h_r V_2$$

$$I_2 = h_f I_1 + h_o V_2$$

(The following convenient alternative subscript notation is recommended by the **IEEE Standards**:

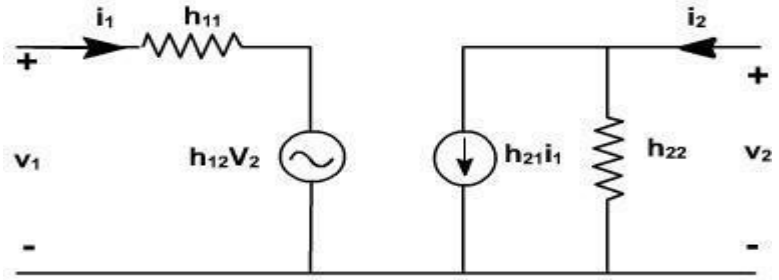
***i*=11= input** ***o* = 22 = output**



***f* =21 = forward transfer *r* = 12 = reverse transfer)**

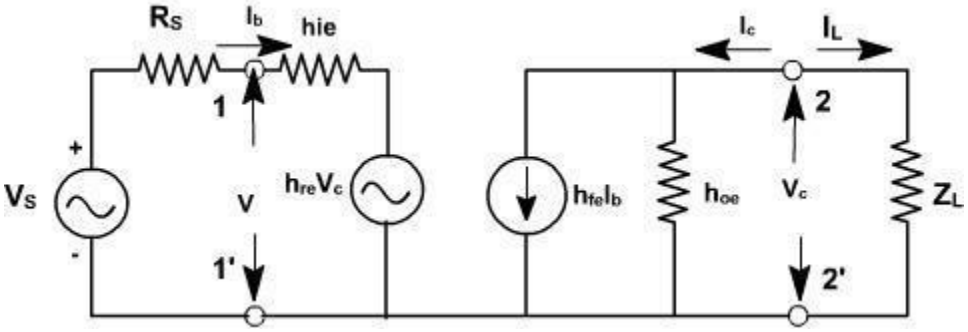
If these parameters are specified for a particular configuration, then suffixes e,b or c are also included, e.g. h_{fe} ,h_{ib} are h parameters of common emitter and common collector amplifiers

Using two equations the generalized model of the amplifier can be drawn as shown in fig. 2.



ANALYSIS OF A TRANSISTOR AMPLIFIER USING H-PARAMETERS:

To form a transistor amplifier it is only necessary to connect an external load and signal source as



indicated in and to bias the transistor properly.

Current gain:

For the transistor amplifier stage, A_i is defined as the ratio of output to input currents.

$$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$

Input impedance:

The impedance looking into the amplifier input terminals (1,1') is the input impedance Z_i

$$Z_i = \frac{V_b}{I_b}$$

$$V_b = h_{ie} I_b + h_{re} V_c$$

$$\frac{V_b}{I_b} = h_{ie} + h_{re} \frac{V_c}{I_b}$$

$$= h_{ie} - \frac{h_{re} I_c Z_L}{I_b}$$

$$\therefore Z_i = h_{ie} + h_{re} A_I Z_L$$

$$= h_{ie} - \frac{h_{re} h_{fe} Z_L}{1 + h_{oe} Z_L}$$

$$\therefore Z_i = h_{ie} - \frac{h_{re} h_{fe}}{Y_L + h_{oe}} \qquad (\text{since } Y_L = \frac{1}{Z_L})$$

Voltage gain:

The ratio of output voltage to input voltage gives the gain of the transistors.

$$A_v = \frac{V_C}{V_b} = -\frac{I_C Z_L}{V_b}$$

$$\therefore A_v = \frac{I_B A_i Z_L}{V_b} = \frac{A_i Z_L}{Z_i}$$

Output Admittance:

$$Y_0 = \left.\frac{I_c}{V_c}\right|_{V_s} = 0$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

$$\frac{I_c}{V_c} = h_{fe} \frac{I_b}{V_c} + h_{oe}$$

when $V_s = 0$, $\quad R_s . I_b + h_{ie} . I_b + h_{re} V_c = 0.$

$$\frac{I_b}{V_c} = -\frac{h_{re}}{R_s + h_{ie}}$$

$$\therefore Y_0 = h_{oe} - \frac{h_{re}\, h_{fe}}{R_s + h_{ie}}$$

Voltage amplification taking into account source impedance (R_S) is given by

$$A_{VS} = \frac{V_c}{V_s} = \frac{V_c}{V_b} * \frac{V_b}{V_S} \qquad \left(V_b = \frac{V_s}{R_s + Z_i} * Z_i\right)$$

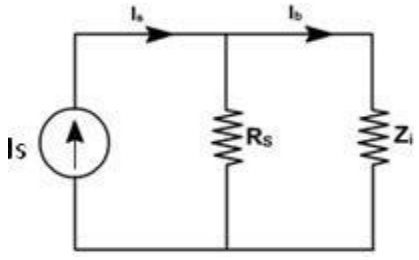
$$= A_V . \frac{Z_i}{Z_i + R_s}$$

$$= \frac{A_i Z_L}{Z_i + R_s}$$

It is defined as

A_v is the voltage gain for an ideal voltage source ($R_v = 0$).

Consider input source to be a current source I_S in parallel with a resistance R_S as shown in <u>fig. 3</u>.



In this case, overall current gain A_{IS} is defined as

$$A_{I_S} = \frac{I_L}{I_s}$$

$$= -\frac{I_c}{I_s}$$

$$= -\frac{I_c}{I_b} * \frac{I_b}{I_s} \qquad \left(I_b = \frac{I_s * R_s}{R_s + Z_i}\right)$$

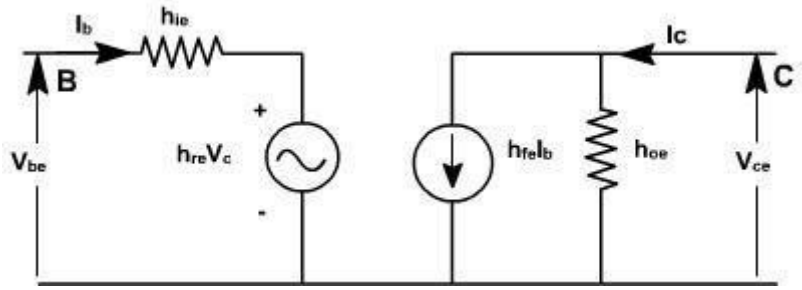
$$= A_I * \frac{R_s}{R_s + Z_i}$$

If $R_s \to \infty, \quad A_{Is} \to A_I$

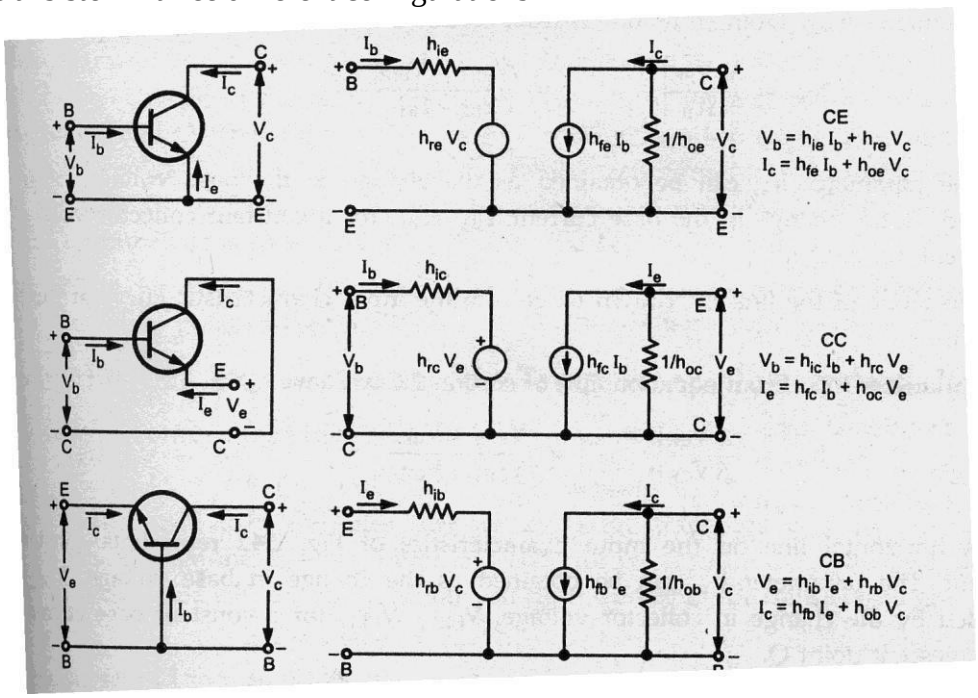
h-parameters:

To analyze multistage amplifier the h-parameters of the transistor used are obtained from manufacture

data sheet. The manufacture data sheet usually provides h-parameter in CE configuration. These parameters may be converted into CC and CB values. For example fig. 4 hrc in terms of CE parameter can be obtained as follows.



hybrid model for transistor in three different configurations



Typical h-parameter values for a transistor

Parameter	CE	CC	CB
h_i	1100 Ω	1100 Ω	22 Ω
h_r	2.5×10^{-4}	1	3×10^{-4}
h_f	50	-51	-0.98
h_o	25 µA/V	25 µA/V	0.49 µA/V

Analysis of a Transistor amplifier circuit using h-parameters

A transistor amplifier can be constructed by connecting an external load and signal source and biasing the transistor properly.

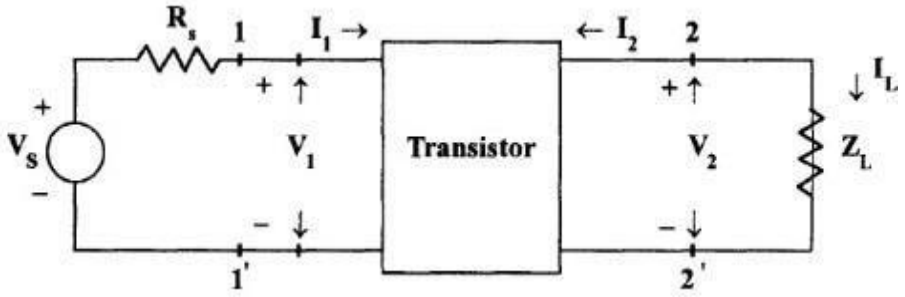


Fig.1.4 Basic Amplifier Circuit

The two port network of Fig. 1.4 represents a transistor in any one of its configuration. It is assumed that h-parameters remain constant over the operating range. The input is sinusoidal and I_1,V_1,I_2 and V_2 are phase quantities.

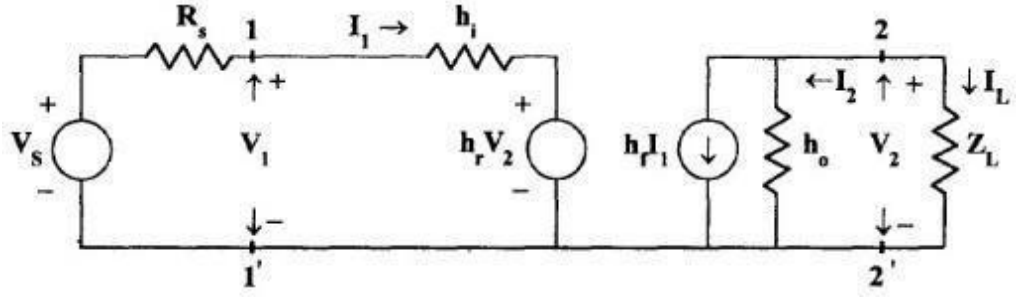


Fig. 1.5 Transistor replaced by its Hybrid Model

Current Gain or Current Amplification (A_i)

For transistor amplifier the current gain A_i is defined as the ratio of output current to input current.

Input Impedance (Z_i)

In the circuit of Fig , R_S is the signal source resistance .The impedance seen when looking into the amplifier terminals (1,1') is the amplifier input impedance Z_i,

$Z_i = V_1 / I_1$

From the input circuit of Fig $V_1 = h_i I_1 +$

$h_r V_2$ $Z_i = (h_i I_1 + h_r V_2) / I_1$

$= h_i + h_r V_2 / I_1$

Substituting

$$V_2 = -I_2 Z_L = A_1 I_1 Z_L$$

$$Z_i = h_i + h_r A_1 I_1 Z_L / I_1$$

$$= h_i + h_r A_1 Z_L$$

Substituting for A_i

$$Z_i = h_i - h_f h_r Z_L / (1 + h_o Z_L)$$

$$= h_i - h_f h_r Z_L / Z_L(1/Z_L + h_o)$$

Taking the Load admittance as

$$Y_L = 1/ Z_L \quad Z_i = h_i - h_f h_r / (Y_L + h_o)$$

Voltage Gain or Voltage Gain Amplification Factor(A_v)

The ratio of output voltage V_2 to input voltage V_1 give the voltage gain of the transistor i.e,

$$A_v = V_2 / V_1$$

Substituting

$$V_2 = -I_2 Z_L = A_1 I_1 Z_L$$

$$A_v = A_1 I_1 Z_L / V_1 = A_i Z_L / Z_i$$

Output Admittance (Y_o)

Y_o is obtained by setting V_S to zero, Z_L to infinity and by driving the output terminals from a generator V_2. If the current V_2 is I_2 then $Y_o = I_2/V_2$ with $V_S=0$ and $R_L = \infty$.

From the circuit of fig

$$I_2 = h_f I_1 + h_o V_2$$

Dividing by V_2,

$$I_2 / V_2 = h_f I_1 / V_2 + h_o$$

With $V_2 = 0$, by KVL in input circuit,

$$R_S I_1 + h_i I_1 + h_r V_2 = 0$$

$$(R_S + h_i) I_1 + h_r V_2 = 0$$

Hence, $I_2 / V_2 = -h_r / (R_S + h_i)$

$$= h_f (-h_r / (R_S + h_i) + h_o$$

$$Y_o = h_o - h_f h_r / (R_S + h_i)$$

The output admittance is a function of source resistance. If the source impedance is resistive then Y_o is real.

Voltage Amplification Factor(A_{vs}) taking into account the resistance (R_s) of the source

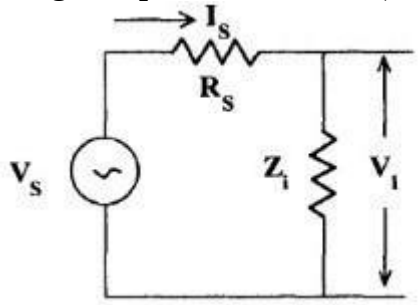


Fig. 5.6 Thevenin's Equivalent Input Circuit

This overall voltage gain A_{vs} is given by

$$A_{vs} = V_2 / V_S = V_2 V_1 / V_1 V_S = A_v V_1 / V_S$$

From the equivalent input circuit using Thevenin's equivalent for the source shown in Fig. 5.6

$$V_1 = V_S Z_i / (Z_i + R_S)$$

$$V_1 / V_S = Z_i / (Z_i + R_S)$$

Then, $A_{vs} = A_v Z_i / (Z_i + R_S)$ Substituting $A_v = A_i Z_L /$

Z_i

$$A_{vs} = A_i Z_L / (Z_i + R_S)$$

$$A_{vs} = A_i Z_L R_S / (Z_i + R_S) R_S$$

$$A_{vs} = A_{is} Z_L / R_S$$

Current Amplification (A_{is}) taking into account the source Resistance(R_S)

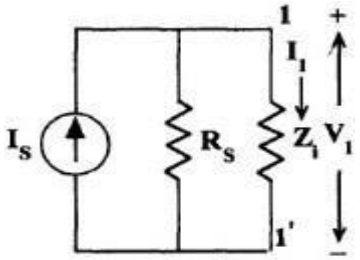


Fig. 1.7 Norton's Equivalent Input Circuit

The modified input circuit using Norton's equivalent circuit for the calculation of A_{is} is shown in Fig. 1.7 Overall Current Gain, $A_{is} = -I_2 / I_S = - I_2 I_1 / I_1 I_S = A_i I_1 / I_S$

From Fig. 1.7 $I_1 = I_S R_S / (R_S + Z_i)$ $I_1 / I_S = R_S / (R_S + Z_i)$

and hence, $A_{is} = A_i R_S / (R_S + Z_i)$

Operating Power Gain (A_P)

The operating power gain A_P of the transistor is defined as

$$A_P = P_2 / P_1 = -V_2 I_2 / V_1 I_1 = A_v A_i = A_i A_i Z_L / Z_i$$

$$A_P = A_i^{\,2} (Z_L / Z_i)$$

NEED FOR TRANSISTOR BIASING:

If the o/p signal must be a faithful reproduction of the i/p signal, the transistor must be operated in active region. That means an operating point has to be established in this region . To establish an operating point (proper values of collector current I_c and collector to emitter voltage V_{CE}) appropriate supply voltages and resistances must be suitably chosen in the ckt. This process of selecting proper supply voltages and resistance for obtaining desired operating point or Q point is called as biasing and the ckt used for transistor biasing is called as biasing ckt.

There are four conditions to be met by a transistor so that it acts as a faithful ampr:

1) Emitter base junction must be forward biased (V_{BE}=0.7Vfor Si, 0.2V for Ge) and collector base junction must be reverse biased for all levels of i/p signal.
2) V_{ce} voltage should not fall below $V_{CE\ (sat)}$ (0.3V for Si, 0.1V for Ge) for any part of the i/p signal. For V_{CE} less than $V_{CE\ (sat)}$ the collector base junction is not probably reverse biased.
3) The value of the signal I_c when no signal is applied should be at least equal to the max. collector current t due to signal alone.
4) Max. rating of the transistor $I_{c(max)}$, $V_{CE\ (max)}$ and $P_{D(max)}$ should not be exceeded at any value of i/p signal.

Consider the fig shown in fig1. If operating point is selected at A, A represents a condition when no bias is applied to the transistor i.e, I_c=0, V_{CE} =0. It does not satisfy the above said conditions necessary for faithful amplification.

Point C is too close to $P_{D(max)}$ curve of the transistor. Therefore the o/p voltage swing in the positive direction is limited.

Point B is located in the middle of active region .It will allow both positive and negative half cycles in the o/p signal. It also provides linear gain and larger possible o/p voltages and currents

Hence operating point for a transistor amplifier is selected to be in the middle of active region.

DC LOAD LINE

Referring to the biasing circuit of fig 4.2a, the values of V_{CC} and R_C are fixed and Ic and V_{CE} are dependent on R_B.

Applying Kirchhoff's voltage law to the collector circuit in fig. 4.2a, we get

$$Vcc = IcRc + Vce$$

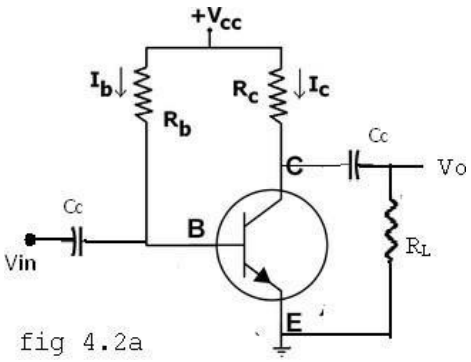


Fig 4.2a CE Amplifier circuit

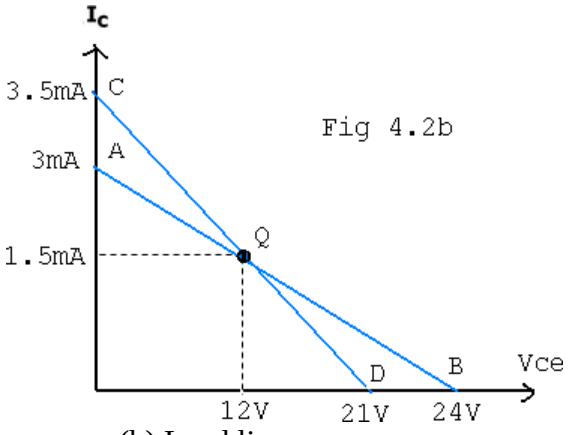


Fig 4.2b

(b) Load line

The straight line represented by AB in fig4.2b is called the dc load line. The coordinates of the end point A are obtained by substituting V_{CE} =0 in the above equation. Then $Ic = \frac{Vcc}{Rc}$. Therefore The coordinates of A are V_{CE} =0 and $Ic = \frac{Vcc}{Rc}$.

The coordinates of B are obtained by substituting Ic=0 in the above equation. Then Vce = Vcc. Therefore the coordinates of B are V_{CE} =Vcc and Ic=0. Thus the dc load line AB can be drawn if the values of Rc and Vcc are known.

As shown in the fig4.2b, the optimum POINT IS LOCATED AT THE MID POINT OF THE MIDWAY BETWEEN a AND b. In order to get faithful amplification, the Q point must be well within the active region of the transistor.

Even though the Q point is fixed properly, it is very important to ensure that the operating point remains stable where it is originally fixed. If the Q point shifts nearer to either A or B, the output voltage and current get clipped, thereby o/p signal is distorted.

In practice, the Q-point tends to shift its position due to any or all of the following three main factors.

1) Reverse saturation current, Ico, which doubles for every 10°C raise in temperature
2) Base emitter Voltage ,VBE, which decreases by 2.5 mV per °C
3) Transistor current gain, h_{FE} or β which increases with temperature.

If base current I_B is kept constant since I_B is approximately equal to Vcc/RB. If the transistor is replaced by another one of the same type, one cannot ensure that the new transistor will have identical parameters as that of the first one. Parameters such as β vary over a range. This results in the variation of collector current Ic for a given I_B. Hence, in the o/p characteristics, the spacing between the curves might increase or decrease which leads to the shifting of the Q-point to a location which might be completely unsatisfactory.

AC LOAD LINE

After drawing the dc load line, the operating point Q is properly located at the center of the dc load line. This operating point is chosen under zero input signal condition of the circuit. Hence the ac load line should also pas through the operating point Q. The effective ac load resistance R_{ac}, is a combination of R_C parallel to R_L i.e. $R_{ac} = R_L \| R_C$. So the slope of the ac load line CQD will be $\left(\frac{-1}{R_{ac}}\right)$. To draw the ac load line, two end points, I.e. $V_{CE(max)}$ and $I_{C(max)}$ when the signal is applied are required.

$V_{CE(\max)} = V_{CEQ} + I_{CQ}R_{ac}$, which locates point D on the Vce axis.

$I_{c(\max))} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$, which locates the point C on the I_C axis.

By joining points c and D, ac load line CD is constructed. As $R_C > R_{ac}$, The dc load line is less steep than ac load line.

STABILITY FACTOR (S):

The rise of temperature results in increase in the value of transistor gain β and the leakage current Ico. So, I_C also increases which results in a shift in operating point. Therefore, The biasing network should be provided with thermal stability. Maintenance of the operating point is specified by S, which indicates the degree of change in operating point due to change in temperature.

The extent to which I_C is stabilized with varying I_C is measured by a stability factor S

$$S = \frac{\partial I_c}{\partial I_{co}} \approx \frac{dI_c}{dI_{co}} \approx \frac{\Delta I_c}{\Delta I_{co}}, \beta \text{ and } I_B \text{ constant}$$

For CE configuration $I_C = \beta I_B + (1+\beta) I_{CO}$

Differentiate the above equation w.r.t I_C , We get

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta) \frac{dI_{co}}{dI_c}$$

$$\therefore \left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta+1)}{S}$$

$$\therefore S = \frac{1+\beta}{1-\beta \frac{dI_B}{dI_C}}$$

S should be small to have better thermal stability.

Stability factor S' and S'':

S' is defined as the rate of change of I_C with V_{BE}, keeping I_C and V_{BE} constant.

$$S' = \frac{\partial I_c}{\partial V_{BE}}$$

S'' is defined as the rate of change of I_C with β, keeping I_{CO} and V_{BE} constant.

$$S'' = \frac{\partial I_c}{\partial \beta}$$

METHODS OF TRANSISTOR BIASING

1) Fixed bias (base bias)

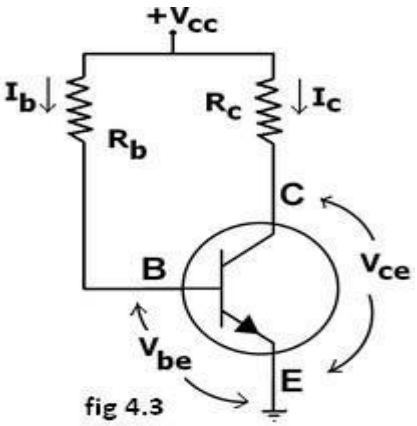


Fig 4.3 Fixed Biasing Circuit

This form of biasing is also called base bias. In the fig 4.3 shown, the single power source (for example, battery) is used for both collector and base of a transistor, although separate batteries can also be used.

In the given circuit, Vcc = IBRB + Vbe

Therefore, IB = (Vcc - Vbe)/RB

Since the equation is independent of current ICR, dIB//dICR =0 and the stability factor is given by the equation….. reduces to

S=1+β

Since β is a large quantity, this is very poor biasing circuit. Therefore in practice the circuit is not used fo biasing.

For a given transistor, Vbe does not vary significantly during use. As Vcc is of fixed value, on selection of R the base current IB is fixed. Therefore this type is called fixed bias type of circuit.

Also for given circuit, Vcc = ICRC + Vce

Therefore, Vce = Vcc - ICRC

Merits:

It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (RB).

A very small number of components are required.

Demerits:

The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.

Changes in Vbe will change IB and thus cause RE to change. This in turn will alter the gain of the stage.

When the transistor is replaced with another one, considerable change in the value ofβ can be expected. Due to this change the operating point will shift.

EMITTER-FEEDBACK BIAS:

The emitter feedback bias circuit is shown in the fig 4.4. The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizes the Q-point. From Kirchhoff's voltage law, the voltage across the base resistor is

VRb = VCC - IeRe - Vbe.

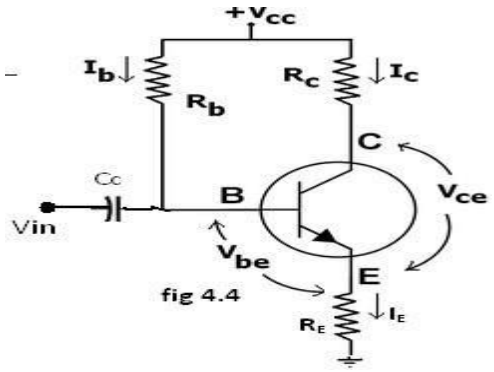


Fig 4.4 Self Biasing Circuit

From Ohm's law, the base current is

Ib = VRb / Rb.

The way feedback controls the bias point is as follows. If Vbe is held constant and temperature increases, emitter current increases. However, a larger Ie increases the emitter voltage Ve = IeRe, which in turn reduces the voltage VRb across the base resistor. A lower base-resistor voltage drop reduces the base current, which results in less collector current because Ic = ß IB. Collector current and emitter current are related by Ic = α Ie with α ≈ 1, so increase in emitter current with temperature is opposed, and operating point is kept stable.

Similarly, if the transistor is replaced by another, there may be a change in IC (corresponding to change in β-value, for example). By similar process as above, the change is negated and operating point kept stable.

For the given circuit,

IB = (VCC - Vbe)/(RB + (β+1)RE).

Merits:

The circuit has the tendency to stabilize operating point against changes in temperature and β-value.

Demerits:

In this circuit, to keep IC independent of β the following condition must be met:

$$I_C = \beta I_B = \frac{\beta(V_{CC} - V_{be})}{R_B + (\beta + 1)R_E} \approx \frac{(V_{CC} - V_{be})}{R_E}$$

which is approximately the case if (β + 1)RE >> RB.

As β-value is fixed for a given transistor, this relation can be satisfied either by keeping RE very large, or making RB very low. If RE is of large value, high VCC is necessary. This increases cost as well as precautions necessary while handling. If RB is low, a separate low voltage supply should be used in the base circuit. Using two supplies of different voltages is impractical. In addition to the above, RE causes ac feedback which reduces the voltage gain of the amplifier.

COLLECTOR TO BASE BIAS OR COLLECTOR FEED-BACK BIAS:

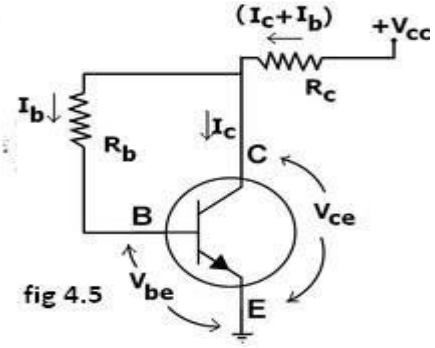


Fig 4.5 Collector to Base Biasing Circuit

This configuration shown in fig 4.5 employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor RB is connected to the collector instead of connecting it to the DC source Vcc. So any thermal runaway will induce a voltage drop across the RC resistor that will throttle the transistor's base current.

From Kirchhoff's voltage law, the voltage V_{R_b}across the base resistor Rb is

$$V_{R_b} = V_{cc} - \overbrace{(I_c + I_b)R_c}^{\text{Voltage drop across } R_c} - \overbrace{V_{be}}^{\text{Voltage at base}}.$$

By the Ebers–Moll model, Ic = βIb, and so

$$V_{R_b} = V_{cc} - (\overbrace{\beta I_b}^{I_c} + I_b)R_c - V_{be} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

From Ohm's law, the base current $I_b = V_{R_b}/R_b$, and so

$$\overbrace{I_b R_b}^{V_{R_b}} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

Hence, the base current Ib is

$$I_b = \frac{V_{cc} - V_{be}}{R_b + (\beta + 1)R_c}$$

If Vbe is held constant and temperature increases, then the collector current Ic increases. However, a larger Ic causes the voltage drop across resistor Rc to increase, which in turn reduces the voltage V_{R_b}across the base resistor Rb. A lower base-resistor voltage drop reduces the base current Ib, which results in less collector current Ic. Because an increase in collector current with temperature is opposed, the operating point is kept stable.

Merits:

Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

Demerits:

In this circuit, to keep Ic independent of β, the following condition must be met:

$$I_c = \beta I_b = \frac{\beta(V_{cc} - V_{be})}{R_b + R_c + \beta R_c} \approx \frac{(V_{cc} - V_{be})}{R_c}$$

which is the case when

$\beta R_c \gg R_b.$

As β-value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping Rc fairly large or making Rb very low. If Rc is large, a high Vcc is necessary, which increases cost as well as precautions necessary while handling. If Rb is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode. The resistor Rb causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

COLLECTOR –EMITTER FEEDBACK BIAS:

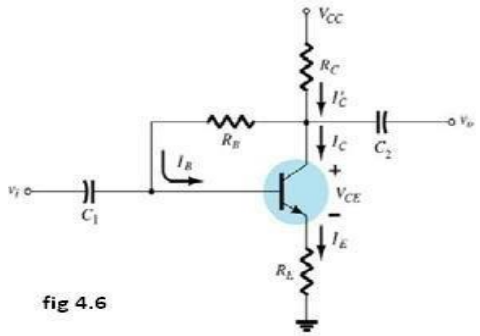


Fig 4.6 Collector-Emitter Biasing Circuit

The above fig4.6 shows the collector –emitter feedback bias circuit that can be obtained by applying both the collector feedback and emitter feedback. Here the collector feedback is provided by connecting a resistance RB from the collector to the base and emitter feedback is provided by connecting an emitter Re from emitter to ground. Both feed backs are used to control collector current and base current IB in the opposite direction to increase the stability as compared to the previous biasing circuits.

VOLTAGE DIVIDER BIAS OR SELF BIAS OR EMITTER BIAS:

The voltage divider as shown in the fig 4.7 is formed using external resistors R1 and R2. The voltage across R2 forward biases the emitter junction. By proper selection of resistors R1 and R2, the operating point of the transistor can be made independent of β. In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor.

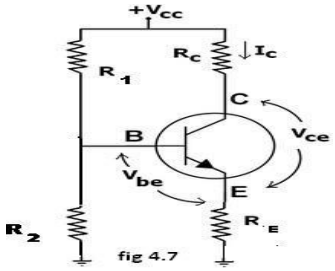


Fig 4.7 Voltage Divider Biasing Circuit

In this circuit the base voltage is given by:

$$V_B = \text{voltage across } R_2 = V_{cc}\frac{R_2}{(R_1+R_2)} - I_B\frac{R_1R_2}{(R_1+R_2)}$$

$$\approx V_{cc}\frac{R_2}{(R_1+R_2)} \text{ provided } I_B << I_2 = V_B/R_2$$

$$V_B = V_{be} + I_E R_E$$

Also For the given circuit,

Let the current in resistor R1 is I1 and this is divided into two parts – current through base and resistor R2. Since the base current is very small so for all practical purpose it is assumed that I1 also flows through R2, so we have

$$I_B = \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2}.$$

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$$V_2 = \frac{V_{CC}}{R_1 + R_2} \cdot R_2$$

Applying KVL in the circuit, we have

$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + I_E R_E$$

$$I_C = \frac{V_2 - V_{BE}}{R_E} \quad \because I_C \cong I_E$$

$$I_C = \frac{\frac{V_{CC}}{R_1 + R_2} \cdot R_2 - V_{BE}}{R_E}$$

$$I_E = \frac{V_2 - V_{BE}}{R_E}$$

It is apparent from above expression that the collector current is independent of ? thus the stability is excellent. In all practical cases the value of VBE is quite small in comparison to the V2, so it can be ignored in the above expression so the collector current is almost independent of the transistor parameters thus this arrangement provides excellent stability.

Again applying KVL in collector circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\because I_C \cong I_E$$

$$\therefore V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

The resistor RE provides stability to the circuit. If the current through the collector rises, the voltage across the resistor RE also rises. This will cause VCE to increase as the voltage V2 is independent of collector current. This decreases the base current, thus collector current increases to its former value.

Stability factor for such circuit arrangement is given by

$$S = \frac{(1+\beta)(R_{eq} + R_E)}{R_{eq} + R_E(1+\beta)}$$

$$R_{eq} = R_1 || R_2$$

$$S = \frac{(1+\beta)\left(1 + \frac{R_{eq}}{R_E}\right)}{\frac{R_{eq}}{R_E} + 1 + \beta}$$

If Req/RE is very small compared to 1, it can be ignored in the above expression thus we have

$$S = \frac{1+\beta}{1+\beta} = 1$$

Which is excellent since it is the smallest possible value for the stability. In actual practice the value of stability factor is around 8-10, since Req/RE cannot be ignored as compared to 1.

Merits:

- Unlike above circuits, only one dc supply is necessary.
- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

In this circuit, to keep IC independent of β the following condition must be met:

$$I_C = \beta I_B = \beta \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2} \approx \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{R_E},$$

which is approximately the case if $(\beta+1)R_E >> R_1 \parallel R_2$

where R1 || R2 denotes the equivalent resistance of R1 and R2 connected in parallel. As β-value is fixed for a given transistor, this relation can be satisfied either by keeping RE fairly large, or making R1||R2 very low. If RE is of large value, high VCC is necessary. This increases cost as well as precautions necessary while handling. If R1 || R2 is low, either R1 is low, or R2 is low, or both are low. A low R1 raises VB closer to VC, reducing the available swing in collector voltage, and limiting how large RC can be made without driving the transistor out of active mode. A low R2 lowers Vbe, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.

AC as well as DC feedback is caused by RE, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage: The circuit's stability and merits as above make it widely used for linear circuits.

MODULE-II
MOSFET CIRCUITS

MOSFET structure and I-V characteristics. MOSFET as a switch. small signal equivalent circuits - gain, input and output impedances, small-signal model and common-source, common-gate and common-drain amplifiers, trans conductance, high frequency equivalent circuit.

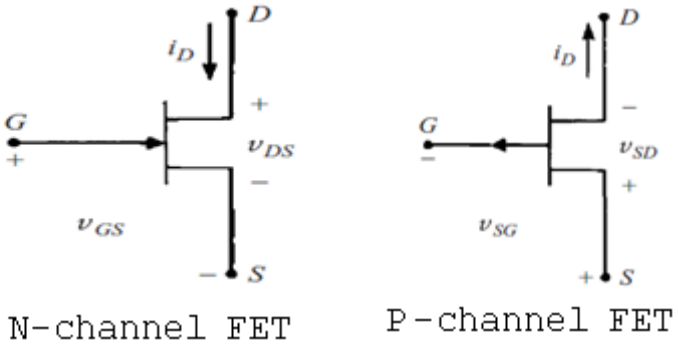
INTRODUCTION

- The Field effect transistor is abbreviated as FET , it is an another semiconductor device like a BJT which can be used as an amplifier or switch.
- The Field effect transistor is a voltage operated device. Whereas Bipolar junction transistor is a current controlled device. Unlike BJT a FET requires virtually no input current.
- This gives it an extremely high input resistance , which is its most important advantage over a bipolar transistor.
- FET is also a three terminal device, labeled as source, drain and gate.
- The source can be viewed as BJT's emitter, the drain as collector, and the gate as the counter part of the base.
- The material that connects the source to drain is referred to as the channel.
- FET operation depends only on the flow of majority carriers ,therefore they are called uni polar devices. BJT operation depends on both minority and majority carriers.
- As FET has conduction through only majority carriers it is less noisy than BJT.
- FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
- FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.
- The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature coefficient at high current levels which leads to thermal breakdown.

6.2 CLASSIFICATION OF FET:

There are two major categories of field effect transistors:
1. Junction Field Effect Transistors
2. MOSFETs

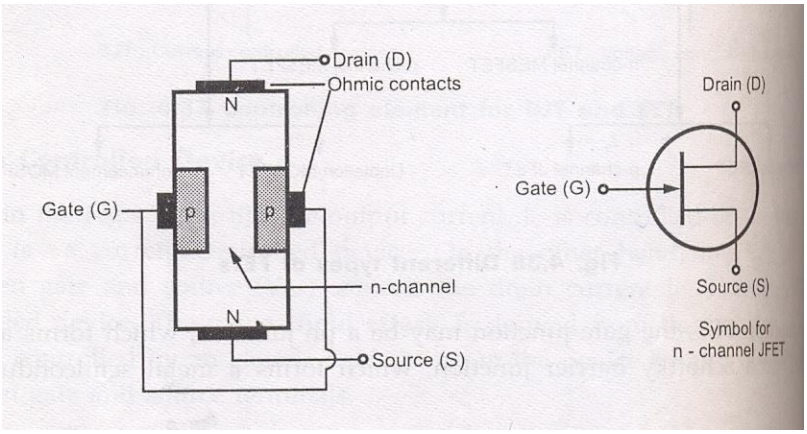
These are further sub divided in to P- channel and N-channel devices.
MOSFETs are further classified in to two types Depletion MOSFETs and Enhancement. MOSFETs
When the channel is of N-type the JFET is referred to as an N-channel JFET, when the channel is of P-type the JFET is referred to as P-channel JFET.
The schematic symbols for the P-channel and N-channel JFETs are shown in the figure.



6.3 CONSTRUCTION AND OPERATION OF N- CHANNEL FET

If the gate is an N-type material, the channel must be a P-type material.

CONSTRUCTION OF N-CHANNEL JFET



A piece of N- type material, referred to as channel has two smaller pieces of P-type material attached to its sides, forming PN junctions. The channel ends are designated as the drain and source . And the two pieces of P-type material are connected together and their terminal is called the gate. Since this channel is in the N-type bar, the FET is known as N-channel JFET.

OPERATION OF N-CHANNEL JFET:-

The overall operation of the JFET is based on varying the width of the channel to control the drain current.

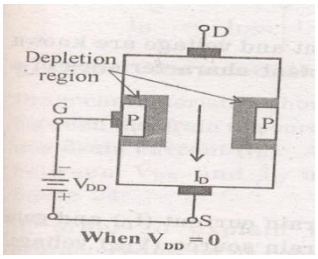
A piece of N type material referred to as the channel, has two smaller pieces of P type material attached to its sites, farming PN –Junctions. The channel's ends are designated the drain and the source. And the two pieces of P type material are connected together and their terminal is called the gate. With the gate terminal not connected and the potential applied positive at the drain negative at the source a drain current Id flows. When the gate is biased negative with respective to the source the PN junctions are reverse biased and depletion regions are formed. The channel is more lightly doped than the P type gate blocks, so the depletion regions penetrate deeply into the channel. Since depletion region is a region depleted of charge carriers it behaves as an Insulator. The result is that the channel is narrowed. Its resistance is increased and Id is reduced. When the negative gate bias voltage is further increased, the depletion regions meet at the center and Id is cut off completely.

There are two ways to control the channel width

- By varying the value of Vgs
- And by Varying the value of Vds holding Vgs constant

1 By varying the value of Vgs :-

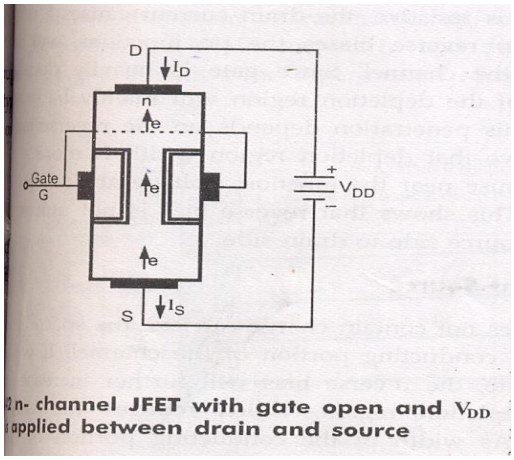
We can vary the width of the channel and in turn vary the amount of drain current. This can be done by varying the value of Vgs. This point is illustrated in the fig below. Here we are dealing with N channel FET. So channel is of N type and gate is of P type that constitutes a PN junction. This PN junction is always reverse biased in JFET operation .The reverse bias is applied by a battery voltage Vgs connected between the gate and the source terminal i.e positive terminal of the battery is connected to the source and negative terminal to gate.



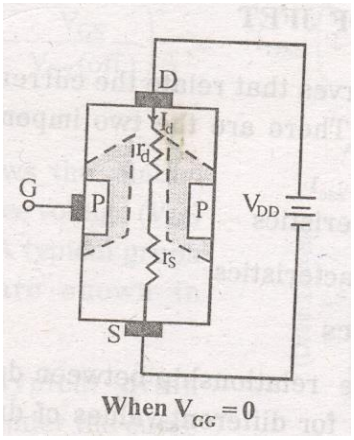
1) When a PN junction is reverse biased the electrons and holes diffuse across junction by leaving immobile ions on the N and P sides , the region containing these immobile ions is known as depletion regions.
2) If both P and N regions are heavily doped then the depletion region extends symmetrically on both sides.
3) But in N channel FET P region is heavily doped than N type thus depletion region extends more in N region than P region.
4) So when no Vds is applied the depletion region is symmetrical and the conductivity becomes Zero. Since there are no mobile carriers in the junction.
5) As the reverse bias voltage is increases the thickness of the depletion region also increases. i.e. the effective channel width decreases .
6) By varying the value of Vgs we can vary the width of the channel.

2 Varying the value of Vds holding Vgs constant :-

- When no voltage is applied to the gate i.e. Vgs=0 , Vds is applied between source and drain the electrons will flow from source to drain through the channel constituting drain current Id .
- With Vgs= 0 for Id= 0 the channel between the gate junctions is entirely open .In response to a small applied voltage Vds , the entire bar acts as a simple semi conductor resistor and the current Id increases linearly with Vds .
- The channel resistances are represented as rd and rs as shown in the fig.



2 n- channel JFET with gate open and V_{DD} applied between drain and source



- This increasing drain current Id produces a voltage drop across rd which reverse biases the gate to source junction,(rd> rs) .Thus the depletion region is formed which is not symmetrical .

- The depletion region i.e. developed penetrates deeper in to the channel near drain and less towards source because Vrd >> Vrs. So reverse bias is higher near drain than at source.
- As a result growing depletion region reduces the effective width of the channel. Eventually a voltage Vds is reached at which the channel is pinched off. This is the voltage where the current Id begins to level off and approach a constant value.
- So, by varying the value of Vds we can vary the width of the channel holding Vgs constant.

When both Vgs and Vds is applied:-

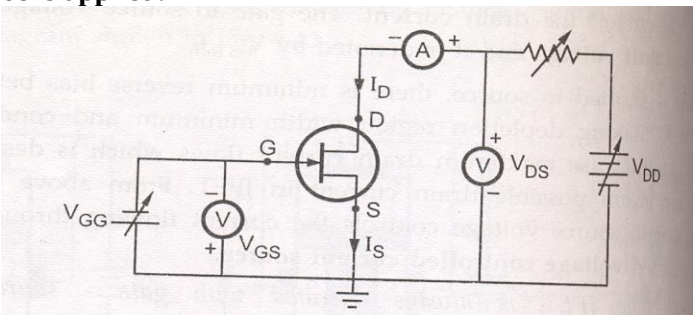
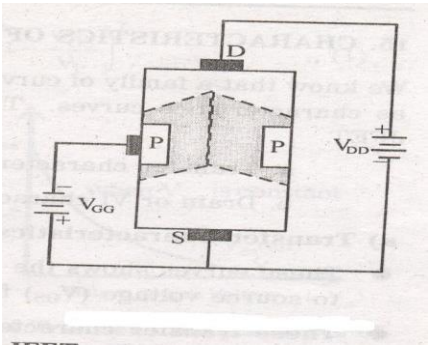


Fig. 4.45 Experimental setup to plot JFET characteristics

It is of course in principle not possible for the channel to close Completely and there by reduce the current Id to Zero for, if such indeed, could be the case the gate voltage Vgs is applied in the direction to provide additional reverse bias

- When voltage is applied between the drain and source with a battery Vdd, the electrons flow from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current Id, its conventional direction is from drain to source.
- The value of drain current is maximum when no external voltage is applied between gate and source and is designated by Idss.



- When Vgs is increased beyond Zero the depletion regions are widened. This reduces the effective width of the channel and therefore controls the flow of drain current through the channel.
- When Vgs is further increased a stage is reached at which to depletion regions touch each other that means the entire channel is closed with depletion region. This reduces the drain current to Zero.

6.4 CHARACTERISTICS OF N-CHANNEL JFET :-

The family of curves that shows the relation between current and voltage are known as characteristic curves.

There are two important characteristics of a JFET.

1) Drain or VI Characteristics
2) Transfer characteristics

- **Drain Characteristics:-**

Drain characteristics shows the relation between the drain to source voltage Vds and

drain current Id. In order to explain typical drain characteristics let us consider the curve with Vgs= 0.V.

1. When Vds is applied and it is increasing the drain current ID also increases linearly up to knee point.
2. This shows that FET behaves like an ordinary resistor. This region is called as ohmic region.
3. ID increases with increase in drain to source voltage. Here the drain current is increased slowly as compared to ohmic region.

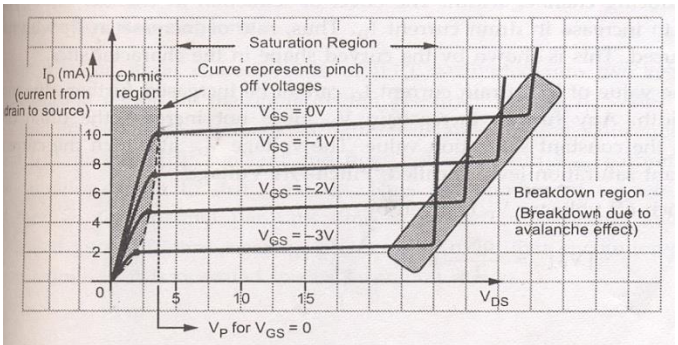


Fig. 4.44 Drain V-I characteristics of n-channel JFET

4) It is because of the fact that there is an increase in VDS .This in turn increases the reverse bias voltage across the gate source junction .As a result of this depletion region grows in size thereby reducing the effective width of the channel.

5) All the drain to source voltage corresponding to point the channel width is reduced to a minimum value and is known as pinch off.

6) The drain to source voltage at which channel pinch off occurs is called pinch off voltage(Vp).

PINCH OFF Region:-

1. This is the region shown by the curve as saturation region.
2. It is also called as saturation region or constant current region. Because of the channel is occupied with depletion region , the depletion region is more towards the drain and less towards the source, so the channel is limited, with this only limited number of carriers are only allowed to cross this channel from source drain causing a current that is constant in this region. To use FET as an amplifier it is operated in this saturation region.
3. In this drain current remains constant at its maximum value IDSS.
4. The drain current in the pinch off region depends upon the gate to source voltage and is given by the relation

$$I_d = I_{dss}\,[1-V_{gs/Vp}]^2$$

This is known as shokley's relation.

BREAKDOWN REGION:-

- The region is shown by the curve .In this region, the drain current increases rapidly as the drain to source voltage is increased.
- It is because of the gate to source junction due to avalanche effect.
- The avalanche break down occurs at progressively lower value of VDS because the reverse bias gate voltage adds to the drain voltage thereby increasing effective voltage across the gate junction

This causes

- The maximum saturation drain current is smaller
- The ohmic region portion decreased.

- It is important to note that the maximum voltage VDS which can be applied to FET is the lowest voltage which causes available break down.

- **TRANSFER CHARACTERISTICS:-**

These curves shows the relationship between drain current ID and gate to source voltage VGS for different values of VDS.

i) First adjust the drain to source voltage to some suitable value , then increase the gate to source voltage in small suitable value.
ii) Plot the graph between gate to source voltage along the horizontal axis and current ID on the vertical axis. We shall obtain a curve like this.

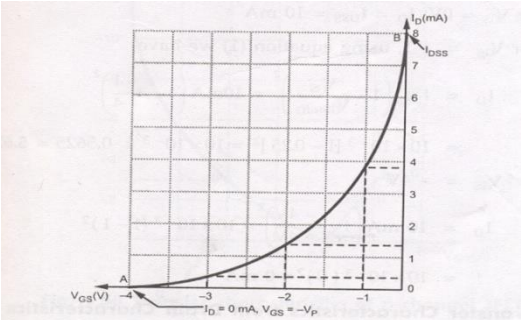


Fig. 4.48 Transfer characteristics of n-channel JFET

iii) As we know that if V_{gs} is more negative curves drain current to reduce . where V_{gs} is made sufficiently negative, I_d is reduced to zero. This is caused by the widening of the depletion region to a point where it is completely closes the channel. The value of V_{gs} at the cutoff point is designed as V_{gsoff}
iv) While the lower end is indicated by a voltage equal to V_{gsoff}
v) If Vg_s continuously increasing , the channel width is reduced , then I_d =0
vi) It may be noted that curve is part of the parabola; it may be expressed as

$I_d=I_{dss}[1-V_{gs}/V_{gsoff}]^2$

DIFFERENCE BETWEEN V_p AND V_{gsoff} –

Vp is the value of V_{gs} that causes the JFET to become constant current component, It is measured at V_{gs} =0V and has a constant drain current of I_d =I_{dss} .Where V_{gsoff} is the value of V_{gs} that reduces I_d to approximately zero.

Why the gate to source junction of a JFET be always reverse biased ?

The gate to source junction of a JFET is never allowed to become forward biased because the gate material is not designed to handle any significant amount of current. If the junction is allowed to become forward biased, current is generated through the gate material. This current may destroy the component. There is one more important characteristic of JFET reverse biasing i.e. J FET ‘s have extremely high characteristic gate input impedance. This impedance is typically in the high mega ohm range. With the advantage of extremely high input impedance it draws no current from the source. The high input impedance of the JFET has led to its extensive use in integrated circuits. The low current requirements of the component makes it perfect for use in ICs. Where thousands of transistors must be etched on to a single piece of silicon. The low current draw helps the IC to remain relatively cool, thus allowing more components to be placed in a smaller physical area.

6.5 JFET PARAMETERS

The electrical behavior of JFET may be described in terms of certain parameters. Such parameters are

obtained from the characteristic curves.

A C Drain resistance(r_d):

It is also called dynamic drain resistance and is the a.c resistance between the drain and source terminal, when the JFET is operating in the pinch off or saturation region. It is given by the ratio of small change in drain to source voltage ΔV_{ds} to the corresponding change in drain current ΔI_d for a constant gate to source voltage V_{gs}.

Mathematically it is expressed as $r_d=\Delta V_{ds}/\Delta I_d$ where V_{gs} is held constant.

TRANCE CONDUCTANCE (g_m):

It is also called forward transconductance . It is given by the ratio of small change in drain current (ΔI_d) to the corresponding change in gate to source voltage (ΔV_{ds})

Mathematically the transconductance can be written as

$$g_m=\Delta I_d/\Delta V_{ds}$$

AMPLIFICATION FACTOR (μ)

It is given by the ratio of small change in drain to source voltage (ΔV_{ds}) to the corresponding change in gate to source voltage (ΔV_{gs})for a constant drain current (I_d).

Thus $\mu=\Delta V_{ds}/\Delta V_{gs}$ when I_d held constant

The amplification factor μ may be expressed as a product of transconductance (g_m)and ac drain resistance (r_d)

$\mu=\Delta V_{ds}/\Delta V_{gs}=g_m\, r_d$

6.6 THE FET SMALL SIGNAL MODEL:-

The linear small signal equivalent circuit for the FET can be obtained in a manner similar to that used to derive the corresponding model for a transistor.

We can express the drain current iD as a function f of the gate voltage and drain voltage V_{ds}.

$I_d=f(V_{gs},V_{ds})$----------(1)

The transconductance g_m and drain resistance r_d:-

If both gate voltage and drain voltage are varied, the change in the drain current is approximated by using taylors series considering only the first two terms in the expansion

$$\Delta i_d=\frac{\partial id}{\partial Vgs}|v_{ds}=\text{constant}\ .\Delta v_{gs}+\frac{\partial id}{\partial Vds}|vgs=\text{constant}\Delta v_{ds}$$

we can write $\Delta i_d=i_d$

$\Delta v_{gs}=v_{gs}$

$\Delta v_{ds}=v_{ds}$

$$I_d=g_m\, vgs\ +\frac{1}{rd}\ Vds\rightarrow(1)$$

Where $g_m=\frac{\partial id}{\partial Vgs}|Vds\cong\frac{\Delta id}{\Delta Vgs}|Vds$

$$g_m=\frac{id}{Vgs}|Vds$$

Is the mutual conductance or transconductance .It is also called as gfs or yfs common source forward conductance .

The second parameter r_d is the drain resistance or output resistance is defined as

$$r_d=\frac{\partial Vds}{\partial id}|_{Vgs}\cong\frac{\Delta vds}{\Delta ids}|_{Vgs}=\frac{Vds}{id}|_{Vgs}$$

$$r_d=\frac{Vds}{id}|_{Vgs}$$

The reciprocal of the rd is the drain conductance gd .It is also designated by Yos and Gos and called the common source output conductance . So the small signal equivalent circuit for FET can be drawn in two different ways.

1.small signal current –source model

2.small signal voltage-source model.

This low frequency model for FET has a Norton's output circuit with a dependent current generator

whose magnitude is proportional to the gate-to –source voltage. The proportionality factor is the transconductance 'g_m'. The output resistance is 'r_d'. The input resistance between the gate and source is infinite, since it is assumed that the reverse biased gate draws no current. For the same reason the resistance between gate and drain is assumed to be infinite.

These small signal models for FET can be used for analyzing the three basic FET amplifier configurations:

1.common source (CS) 2.common drain (CD) or source follower

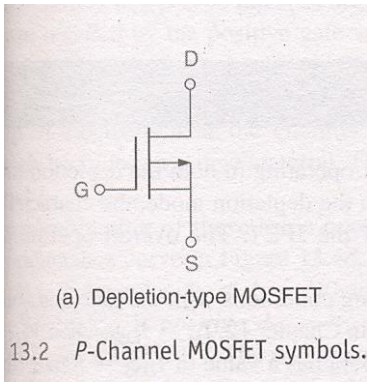
3. common gate(CG).

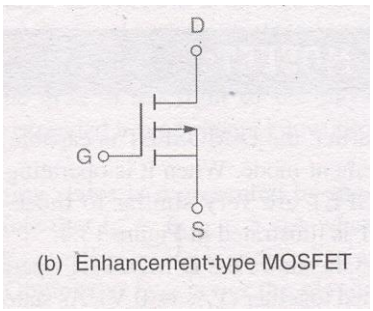
(a)Small Signal Current source model for FET (b)Small Signal voltage source model for FET

6.7 MOSFET:-

We now turn our attention to the insulated gate FET or metal oxide semi conductor FET which is having the greater commercial importance than the junction FET.

Most MOSFETS however are triodes, with the substrate internally connected to the source. The circuit symbols used by several manufacturers are indicated in the Fig below.





(a) Depletion type MOSFET (b) Enhancement type MOSFET

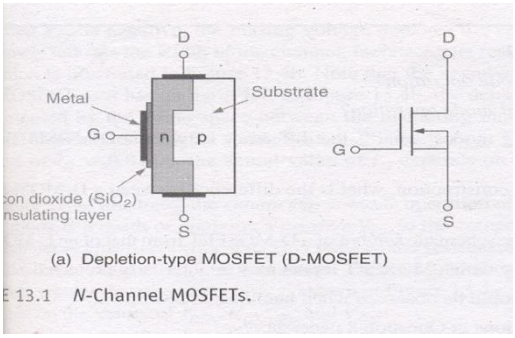
Both of them are P- channel

Here are two basic types of MOSFETS

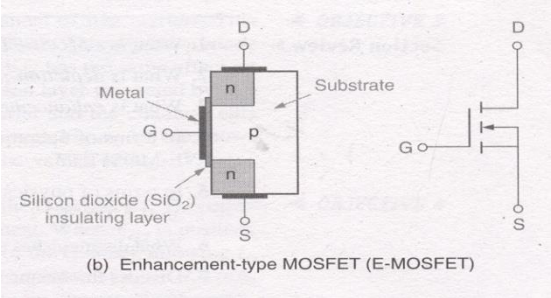
(1) Depletion type (2) Enhancement type MOSFET.

D-MOSFETS can be operated in both the depletion mode and the enhancement mode. E MOSFETS are restricted to operate in enhancement mode. The primary difference between them is their physical construction.

The construction difference between the two is shown in the fig given below.



As we can see the D MOSFET have physical channel between the source and drain terminals(Shaded area)



(b) Enhancement-type MOSFET (E-MOSFET)

The E MOSFET on the other hand has no such channel physically. It depends on the gate voltage to form a channel between the source and the drain terminals.

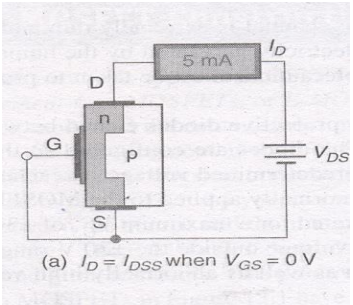
Both MOSFETS have an insulating layer between the gate and the rest of the component. This insulating layer is made up of SIO_2 a glass like insulating material. The gate material is made up of metal conductor .Thus going from gate to substrate, we can have metal oxide semi conductor which is where the term MOSFET comes from. Since the gate is insulated from the rest of the component, the MOSFET is sometimes referred to as an insulated gate FET or IGFET. The foundation of the MOSFET is called the substrate. This material is represented in the schematic symbol by the center line that is connected to the source. In the symbol for the MOSFET, the arrow is placed on the substrate. As with JFET an arrow pointing in represents an N-channel device, while an arrow pointing out represents p-channel device.

CONSTRUCTION OF AN N-CHANNEL MOSFET:-

The N- channel MOSFET consists of a lightly doped p type substance into which two heavily doped n+ regions are diffused as shown in the Fig. These n+ sections, which will act as source and drain. A thin layer of insulation silicon dioxide (SIO_2) is grown over the surface of the structure, and holes are cut into oxide layer, allowing contact with the source and drain. Then the gate metal area is overlaid on the oxide, covering the entire channel region. Metal contacts are made to drain and source and the contact to the metal over the channel area is the gate terminal. The metal area of the gate, in conjunction with the insulating dielectric oxide layer and the semiconductor channel, forms a parallel plate capacitor. The insulating layer of sio2
Is the reason why this device is called the insulated gate field effect transistor. This layer results in an extremely high input resistance (10 10 to 10power 15ohms) for MOSFET.

6.7.1 DEPLETION MOSFET

The basic structure of D –MOSFET is shown in the fig. An N-channel is diffused between source and drain with the device an appreciable drain current IDSS flows foe zero gate to source voltage, Vgs=0.

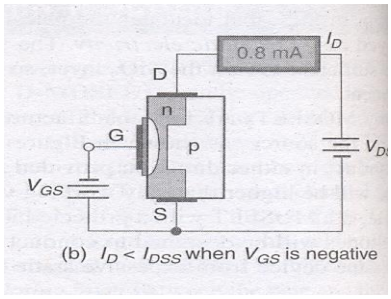


(a) $I_D = I_{DSS}$ when $V_{GS} = 0$ V

Depletion mode operation:-

1. The above fig shows the D-MOSFET operating conditions with gate and source terminals shorted together(VGS=0V)
2. At this stage ID= IDSS where VGS=0V, with this voltage VDS, an appreciable drain current IDSS flows.
3. If the gate to source voltage is made negative i.e. VGs is negative .Positive charges are induced in the channel through the SIO2 of the gate capacitor.
4. Since the current in a FET is due to majority carriers(electrons for an N-type material) , the induced positive charges make the channel less conductive and the drain current drops as Vgs is made more negative.

5. The re distribution of charge in the channel causes an effective depletion of majority carriers , which accounts for the designation depletion MOSFET.
6. That means biasing voltage Vgs depletes the channel of free carriers This effectively reduces the width of the channel , increasing its resistance.
7. Note that negative Vgs has the same effect on the MOSFET as it has on the JFET.

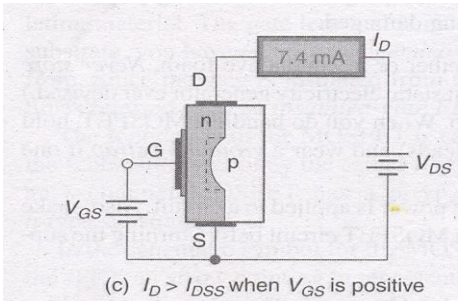


(b) $I_D < I_{DSS}$ when V_{GS} is negative

8. As shown in the fig above, the depletion layer generated by Vgs (represented by the white space between the insulating material and the channel) cuts into the channel, reducing its width. As a result ,Id<Idss. The actual value of ID depends on the value of Idss,Vgs(off) and Vgs.

Enhancement mode operation of the D-MOSFET:-

- This operating mode is a result of applying a positive gate to source voltage Vgs to the device.
- When Vgs is positive the channel is effectively widened. This reduces the resistance of the channel allowing ID to exceed the value of IDSS
- When Vgs is given positive the majority carriers in the p-type are holes. The holes in the p type substrate are repelled by the +ve gate voltage.
- At the same time, the conduction band electrons (minority carriers) in the p type material are attracted towards the channel by the +gate voltage.
- With the build up of electrons near the channel , the area to the right of the physical channel effectively becomes an N type material.
- The extended n type channel now allows more current, Id> Idss



(c) $I_D > I_{DSS}$ when V_{GS} is positive

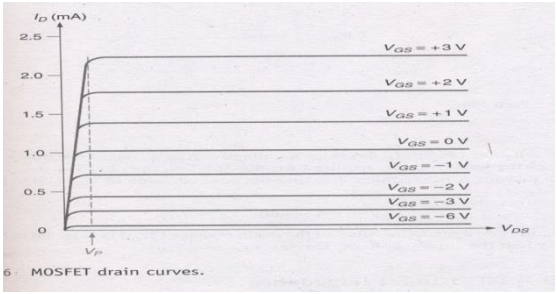
FIGURE 13.4 D-MOSFET operation.

Characteristics of Depletion MOSFET:-

The fig. shows the drain characteristics for the N channel depletion type MOSFET

1) The curves are plotted for both Vgs positive and Vgs negative voltages
2) When Vgs=0 and negative the MOSFET operates in depletion mode when Vgs is positive ,the MOSFET operates in the enhancement mode.
3) The difference between JFET and D MOSFET is that JFET does not operate for positive values of Vgs.
4) When Vds=0, there is no conduction takes place between source to drain, if Vgs<0 and Vds>0 then Id increases linearly.
5) But as Vgs,0 induces positive charges holes in the channel, and controls the channel width. Thus the conduction between source to drain is maintained as constant, i.e. Id is constant.

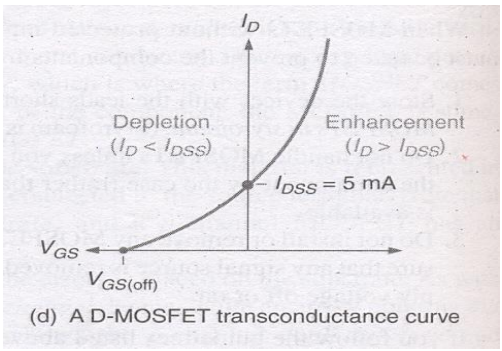
6) If Vgs>0 the gate induces more electrons in channel side, it is added with the free electrons generated by source. again the potential applied to gate determines the channel width and maintains constant current flow through it as shown in Fig



6 MOSFET drain curves.

TRANSFER CHARACTERISTICS:-

The combination of 3 operating states i.e. Vgs=0V, VGs<0V, Vgs>0V is represented by the D MOSFET transconductance curve shown in Fig.

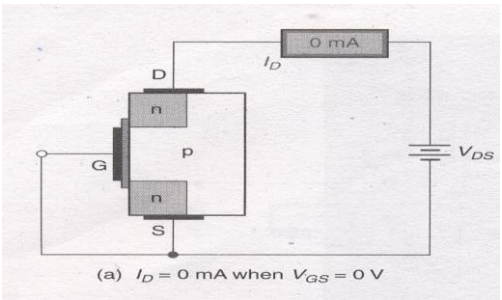


(d) A D-MOSFET transconductance curve

- Here in this curve it may be noted that the region AB of the characteristics similar to that of JFET.
- This curve extends for the positive values of Vgs
- Note that Id=Idss for Vgs=0V when Vgs is negative,Id< Idss when Vgs= Vgs(off) ,Id is reduced to approximately omA.Where Vgs is positive Id>Idss.So obviously Idss is not the maximum possible value of Id for a MOSFET.
- The curves are similar to JFET so thet the D MOSFET have the same transconductance equation.

6.7.2 E-MOSFETS

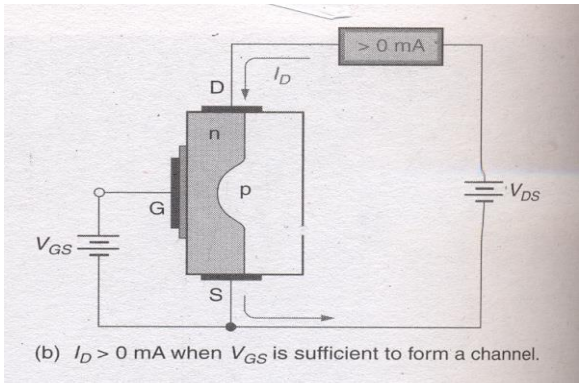
The E MOSFET is capable of operating only in the enhancement mode. The gate potential must be positive w.r.t to source.



(a) $I_D = 0$ mA when $V_{GS} = 0$ V

- ✓ when the value of Vgs=0V, there is no channel connecting the source and drain materials.
- ✓ As aresult , there can be no significant amount of drain current.

- ✓ When Vgs=0, the Vdd supply tries to force free electrons from source to drain but the presence of p-region does not permit the electrons to pass through it. Thus there is no drain current at Vgs=0,
- ✓ If Vgs is positive, it induces a negative charge in the p type substrate just adjacent to the SIO2 layer.
- ✓ As the holes are repelled by the positive gate voltage, the minority carrier electrons attracted toward this voltage. This forms an effective N type bridge between source and drain providing a path for drain current.
- ✓ This +ve gate voltage forma a channel between the source and drain.
- ✓ This produces a thin layer of N type channel in the P type substrate. This layer of free electrons is called N type inversion layer.



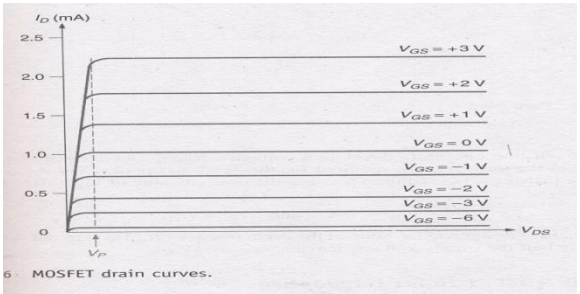
(b) $I_D > 0$ mA when V_{GS} is sufficient to form a channel.

- ✓ The minimum Vgs which produces this inversion layer is called threshold voltage and is designated by Vgs(th).This is the point at which the device turns on is called the threshold voltage Vgs(th)
- ✓ When the voltage Vgs is <Vgs (th) no current flows from drain to source.
- ✓ How ever when the voltage Vgs > Vgs (th) the inversion layer connects the drain to source and we get significant values of current.

CHARACTERISTICS OF E MOSFET:-

- **DRAIN CHARACTERISTICS**

The volt ampere drain characteristics of an N-channel enhancement mode MOSFET are given in the fig



6 · MOSFET drain curves.

- **TRANSFER CHARACTERISTICS:-**

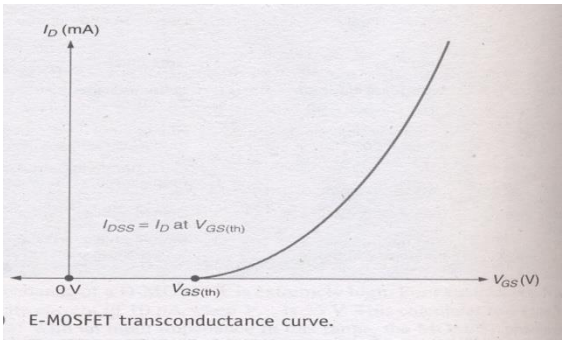
- The current Idss at Vgs≤ 0 is very small beinf of the order of a few nano amps.
- As Vgs is made +ve , the current Id increases slowly at forst, and then much more rapidly with an increase in Vgs.
- The standard transconductance formula will not work for the E MOSFET.
- To determine the value of ID at a given value of VGs we must use the following relation

$$Id = K[V_{gs} - V_{gs(Th)}]^2$$

Where K is constant for the MOSFET . found as

$$K=\frac{Id(on)}{[vgs(on)-Vgs(Th)]2}$$

From the data specification sheets, the 2N7000 has the following ratings.
Id(on)= 75mA(minimum).
And Vgs(th)=0.8(minimum)



E-MOSFET transconductance curve.

6.8 APPLICATION OF MOSFET

One of the primary contributions to electronics made by MOSFETs can be found in the area of digital (computer electronics). The signals in digital circuits are made up of rapidly switching dc levels. This signal is called as a rectangular wave ,made up of two dc levels (or logic levels). These logic levels are 0V and +5V. A group of circuits with similar circuitry and operating characteristics is referred to as a logic family. All the circuits in a given logic family respond to the same logic levels, have similar speed and power-handling capabilities , and can be directly connected together. One such logic family is complementary MOS (or CMOS) logic. This logic family is made up entirely of MOSFETs.

Small Signal Model, Analysis of CS, CD, CG JFET Amplifiers. Basic Concepts of MOSFET Amplifiers.

INTRODUCTION

Field Effect Transistor (FET) amplifiers provide an excellent voltage gain and high input impedance. Because of high input impedance and other characteristics of JFETs they are preferred over BJTs for certain types of applications.

There are 3 basic FET circuit configurations:

i)Common Source ii)Common Drain iii)Common Gain

Similar to BJT CE,CC and CB circuits, only difference is in BJT large output collector current is controlled by small input base current whereas FET controls output current by means of small input voltage. In both the cases output current is controlled variable.

FET amplifier circuits use voltage controlled nature of the JFET. In Pinch off region, I_D depends only on V_{GS}.

7.1 Common Source (CS) Amplifier

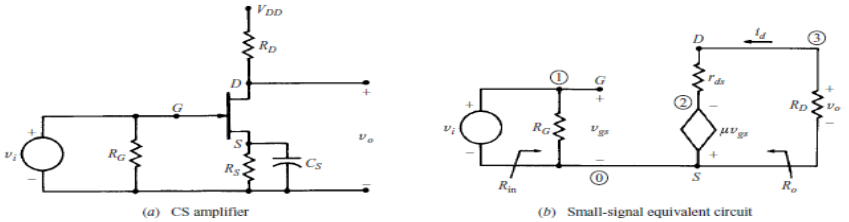


Fig. 7.1 (a) CS Amplifier (b) Small-signal equivalent circuit

A simple Common Source amplifier is shown in Fig. 7.1(a) and associated small signal equivalent circuit using voltage-source model of FET is shown in Fig. 7.1(b)

Voltage Gain

Source resistance (R_S) is used to set the Q-Point but is bypassed by C_S for mid-frequency operation. From the small signal equivalent circuit ,the output voltage

$$V_O = -R_D \mu V_{gs}(R_D + r_d)$$

Where $V_{gs} = V_i$, the input voltage,

Hence, the voltage gain,

$$A_V = V_O / V_i = -R_D \mu (R_D + r_d)$$

Input Impedance

From Fig. 7.1(b) Input Impedance is

$$Z_i = R_G$$

For voltage divider bias as in CE Amplifiers of BJT

$$R_G = R_1 \parallel R_2$$

Output Impedance

Output impedance is the impedance measured at the output terminals with the input voltage $V_I = 0$

From the Fig. 7.1(b) when the input voltage $V_i = 0$, $V_{gs} = 0$ and hence

$$\mu V_{gs} = 0$$

The equivalent circuit for calculating output impedance is given in Fig. 7.2.

Output impedance $Z_o = r_d \parallel R_D$

Normally r_d will be far greater than R_D . Hence $Z_o \approx R_D$

7.2 Common Drain Amplifier

A simple common drain amplifier is shown in Fig. 7.2(a) and associated small signal equivalent circuit using the voltage source model of FET is shown in Fig. 7.2(b).Since voltage V_{gd} is more easily determined than V_{gs}, the voltage source in the output circuit is expressed in terms of V_{gs} and Thevenin's theorem.

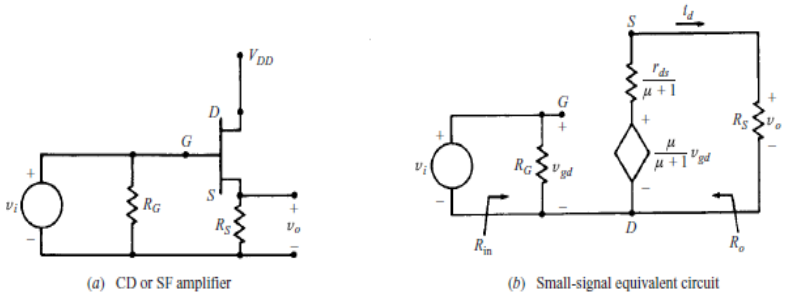


Fig. 7.2 (a)CD Amplifier (b)Small-signal equivalent circuit

Voltage Gain

The output voltage,

$$V_O = R_S \mu V_{gd} / (\mu + 1) R_S + r_d$$

Where $V_{gd} = V_i$ the input voltage.

Hence, the voltage gain,

$$A_v = V_O / V_i = R_S \mu / (\mu + 1) R_S + r_d$$

Input Impedance

Input Impedance $Z_i = R_G$

Output Impedance

From Fig. 7.2(b), Output impedance measured at the output terminals with input voltage $V_i = 0$ can be calculated from the following equivalent circuit.

As $V_i = 0$: $V_{gd} = 0$: $\mu v_{gd} / (\mu + 1) = 0$

Output Impedance

$$Z_O = r_d / (\mu + 1) \parallel R_S \qquad \text{When } \mu \gg 1$$

$$Z_O = (r_d / \mu) \parallel R_S = (1/g_m) \parallel R_S$$

MODULE-III

MULTISTAGE AND POWER AMPLIFIERS

Classification of Amplifiers, Distortion in amplifiers, Different coupling schemes used in amplifiers, Frequency response and Analysis of multistage amplifiers, Cascade amplifier, Darlington pair.

Transistor at High Frequency: *Hybrid - model of Common Emitter transistor model, f_α, β and unity gain bandwidth, Gain band width product. Differential Amplifiers, Power amplifiers - Class A, Class B, Class C, Class AB.*

In order to realize the function of amplification, the transformer may appear to be a potential device. However, in a transformer, though there is magnification of input voltage or current, the power required for the load has to be drawn from the source driving the input of the transformer. The output power is always less than the input power due to the losses in the core and windings. The situation in amplification is that the input source is not capable of supplying appreciable power. Hence the functional block meant for amplification should not draw any power from the input source but should deliver finite out power to the load.

Thus the functional block required should have input power

$$P_i = V_i I_i = 0$$

And give the output

$$P_0 = V_0 I_0 = \text{finite}$$

Such a functional block is called an ideal amplifier, which is shown in Fig.1 below.

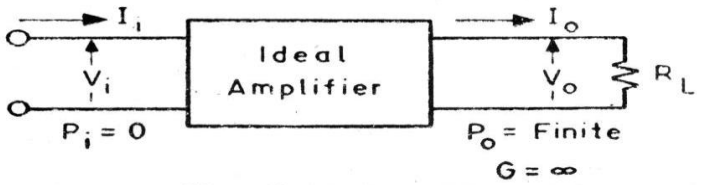


Fig. 1 Ideal amplifier

Power gain is $G = P_0/P_i$

The power gain of an ideal amplifier being infinite may sound like witchcraft in that something can be produced from nothing. The real fact is that the ideal amplifier requires dc input power. It converts dc power to ac power without any demand on the signal source to supply the power for the load.

CLASSIFICATION OF AMPLIFIERS:

Amplifiers are classified in many ways based on different criteria as given below.

I In terms of frequency range:

1. DC amplifiers. (0 Hz to 20 Hz)
2. Audio amplifiers (20 Hz to 20 KHz)
3. Radio frequency amplifiers (Few KHz to hundreds of KHz)
4. Microwave amplifiers (In the range of GHz)
5. Video amplifiers (Hundreds of GHz)

II **In terms of signal strength:**

1. Small signal amplifiers.
2. Large signal mplifiers

III. In terms of coupling:

1. Direct coupling.
2. Resistance – capacitance (RC) coupling.
3. Transformer coupling.

IV. In terms of parameter:

1. Voltage amplifiers.
2. Current amplifiers.
3. Power amplifiers.

V. In terms of biasing condition:

1. Class A amplifier
2. Class B amplifier
3. Class AB amplifier
4. Class C amplifier.

VI. In terms of tuning:

1. Single tuned amplifier
2. Double tuned amplifier
3. Stagger tuned amplifier.

DECIBEL NOTATION:

The power gain of an amplifier is expressed as the ratio of the output power to the input power. When we have more than one stage of amplification i.e. when the output of one stage becomes the input to the next stage, the overall gain has to be obtained by multiplying the gains of the

individual stages. When large numbers are involved, this calculation becomes cumbersome. Also, when we have passive coupling networks between amplifier stages, there will be attenuation of the signal that is gain less than unity. To find the overall gain of a typical multistage amplifier such as the one given below.

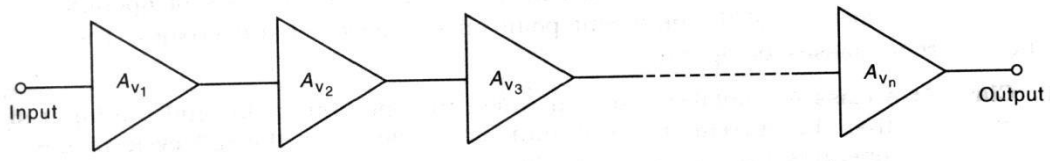


Fig. Cascaded amplifiers

We have to multiply the various gains and attenuations. Moreover, when we wish to plot the gain of an amplifier versus frequency, using large numbers for plotting is not convenient. Hence it has been the practice to use a new unit called the decibel (usually abbreviated as dB) for measuring the power gain of a four terminal network. The power gain in decibels is given by

$$G = 10 \log_{10} P_0 / P_i \text{ dB}$$

This new notation is also significant in the field of acoustics as the response of the human ear to sound intensity is found to be following this logarithmic pattern. The overall gain in decibel notation can be obtained for the amplifier gain of the figure1 by simply adding the decibel gains of the individual networks. If any network attenuates the signal, the gain will be less than the unity and the decibel gain will be negative. Thus the overall gain for the amplifier chain shown above is given by

$$\text{Overall gain} = 10 - 6 + 30 - 10 + 20 = 44 \text{ dB}$$

The absolute power level of the output of an amplifier is sometimes specified in dBm, i.e. decibels with reference to a standard power power level, which is usually, 1 Mw dissipated in a 600 □ load. Therefore, if an amplifier has 100 Mw, its power level in dBm is equal to 10 log 100/1 = 20 dBm.

MULTISTAGE AMPLIFIERS:

In real time applications, a single amplifier can't provide enough output. Hence, two or more amplifier stages are cascaded (connected one after another) to provide greater output Such an arrangement is known as multistage amplifier Though the basic purpose of this arrangement is increase the overall gain, many new problems as a consequence of this, are to be taken care. For e.g. problems such as the interaction between stages due to impedance mismatch, cumulative hum & noise etc.

DISTORTION IN AMPLIFIERS:

In any amplifier, ideally the output should be a faithful reproduction of the input. This is called fidelity. Of course there could be changes in the amplitude levels. However in practice this never happens. The output waveform tends to be different from the input. This is called as the distortion. The distortion may arise either from the inherent non – linearity in the transistor characteristics or from the influence of the associated circuit.

The distortions are classified as:

1. Non – linear or amplitude distortion
2. Frequency distortion
3. Phase distortion
4. Inter modulation distortion

NON – LINEAR DISTORTION:

This is produced when the operation is over the non-linear part of the transfer characteristics of the transistor. (A plot between output v/s input is called as the transfer characteristics). Since the amplifier amplifies different parts of the input differently. For example, there can be compression of the positive half cycle and expansion of the negative half cycle. Sometimes, the waveform can become clipped also. (Flattening at the tips). Such a deviation from linear amplification produces frequencies in the output, which are not originally present in the output. Harmonics (multiples) of the input signal frequency are present in the output. The percentage harmonic distortion for the n^{th}

Harmonic is given by

$$D_n = \frac{A_n \text{ (amplitude of the n the harmonic)}}{A_1 \text{(amplitude of the fundamental)}} \times 100\%$$

And the total harmonic distortion by

$$D_T = \sqrt{D_2^2 + D_3^2 + \dots + D_n^2}$$

Where D_2, D_3 □ □ □ □ are harmonic components.

A distortion factor meter measures the total distortion. The spectrum or wave analyzer can be used to measure the amplitude of each harmonic.

FREQUENCY DISTORTION:

A practical signal is usually complex (containing many frequencies). Frequency distortion occurs when the different frequency components in the input signal are amplified differently. This is due to the various frequency dependent reactances (capacitive & inductive) present in the circuit or the active devices (BJT or FET).

PHASE DISTRIBUTION:

This occurs due to different frequency components of the input signal suffering different phase shifts. The phase shifts are also due to reactive effects and the active devices. This causes problems in TV picture reception. To avoid this amplifier phase shift should be proportional to the frequency.

INTERMODULATION DISTORTION:

The harmonics introduced in the amplifier can combine with each other or with the original frequencies to produce new frequencies to produce new frequencies that are not harmonics of the fundamental. This is called inter modulation distortion. This distortion results in unpleasant hearing.

FREQUENCY RESPONSE OF AN AMPLIFIER:

Frequency response of an amplifier is a plot between gain & frequency. If the gain is constant (same) for all frequencies of the input signal, then this plot would be a flat line. But this never happens in practice.

As explained earlier, there are different reactive effects present in the amplifier circuit and the active devices used. Infact there are external capacitors used for blocking, capacitors etc. Also, in tuned amplifiers, resonant LC circuits are connected in the collector circuits of the amplifier to get narrow band amplification around the resonant frequencies.

Fig below shows a frequency response of a typical amplifier.

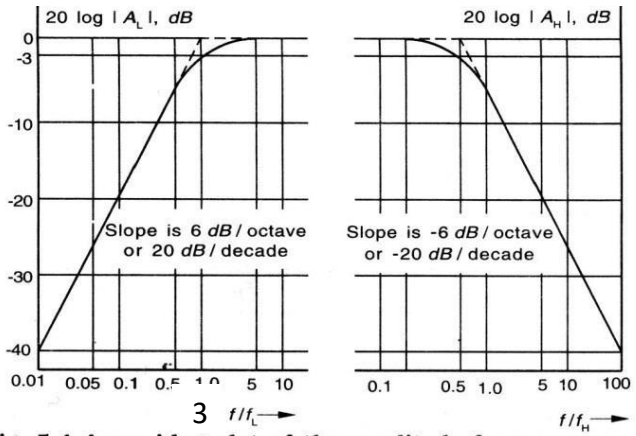


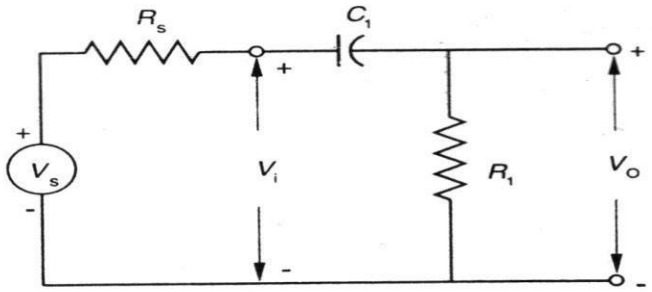
Fig. 5.4 A semi-log plot of the amplitude frequency-response (Bode) characteristic of an *RC* coupled amplifier

Where A_{mid} = mid band voltage gain (in dB)

f_L = Lower cut – off frequency. (in Hz)

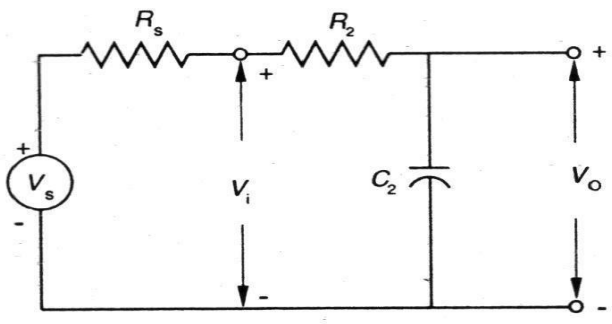
f_H = Upper cut - off frequency (in Hz)

Usually the frequency response of an amplifier is divided into three regions. (i) The mid band region or flat region, over which the gain is constant (ii) The lower frequency region. Here the amplifier behaves like a high pass filter, which is shown below.



(a) High-pass circuit

At high frequencies, the reactance of C_1 will be small & hence it acts as a short without any attenuation (reduction in signal voltage) (iii) In the high frequency region above mid band, the circuit often behaves like the low pass filter as shown below.



(b) Low-pass circuit

As the frequency is increased, the reactance of C_2 decreases. Hence more voltage is dropped across Rs and less is available at the output. Thus the voltage gain of the amplifier decreases at high frequencies.

LOW FREQUENCY RESPONSE:

In the frequency below the mid band, the High pass filter as shown above can approximate the amplifier. This is equal to 3 dB in log scale. For higher frequencies $f >> f_L$, A_L tends to unity. Hence, the magnitude of A_{VL} falls of to 70.7 % of the mid band value at $f = f_L$, Such a frequency is called the lower cut-off or lower 3 dB frequency.

HIGH FREQUENCY RESPONSE:

In the high frequency region, above the mid band , the amplifier stage can be approximated by the low pass circuit.

FREQUENCY RESPONSE PLOTS:

The gain & phase plots versus frequency can be approximately sketched by using straight-line segments called asymptotes. Such plots are called Bode plots. Being in log scale, these plots are very convenient for evaluation of cascaded amplifiers.

BANDWIDTH:

The range of frequencies from f_L to f_H is called the bandwidth of the amplifier. The product of mid band gain and the 3dB Bandwidth of an amplifier is called the Gain-bandwidth product. It is figure of merit or performance measure for the amplifier.

RC COUPLED AMPLIFIER:

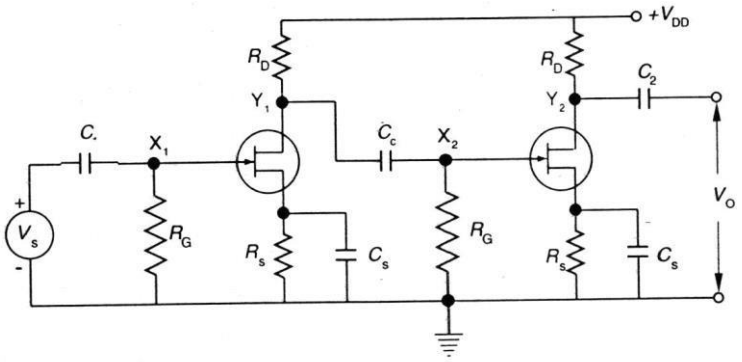


Fig 2 **Two-stage *RC* coupled amplifier with FETs**

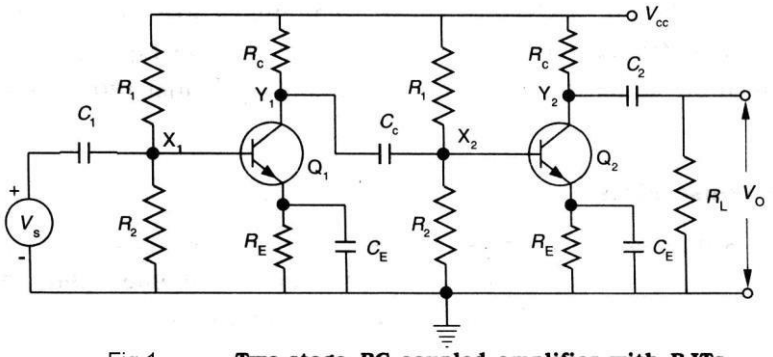


Fig 1 **Two-stage *RC* coupled amplifier with BJTs**

Fig. (1) above shows a two stage RC coupled CE amplifier using BJTs where as fig.(2) shows the FET version. The resistors R_C & R_B (= R_1R_2 / (R_1 + R_2) and capacitors C_C form the coupling network. Because of this, the arrangement is called as RC coupled amplifier. The bypass capacitors C_E (= C_S) are used to prevent loss of amplification due to –ve feedback. The junction capacitance C_j should be taken into account when high frequency operation is considered.

When an ac signal is applied to the input of the I stage, it is amplified by the active device (BJT or FET) and appears across the collector resistor R_C / drain resistor R_D. this output signal is connected to the input of the second stage through a coupling capacitor C_C. The second stage doesn't further amplification of the signal. In this way, the cascaded stages give a large output & the overall gain is equal to the product of this individual stage gains.

ANALYSIS OF TWO STAGE RC COUPLED AMPLIFIER:

This analysis is done using h parameter model. Assuming all capacitors are arbitrarily large and act as ac short circuits across R_E. The dc power supply is also replaced by a short circuit. Their h parameter approximate models replace the transistors.

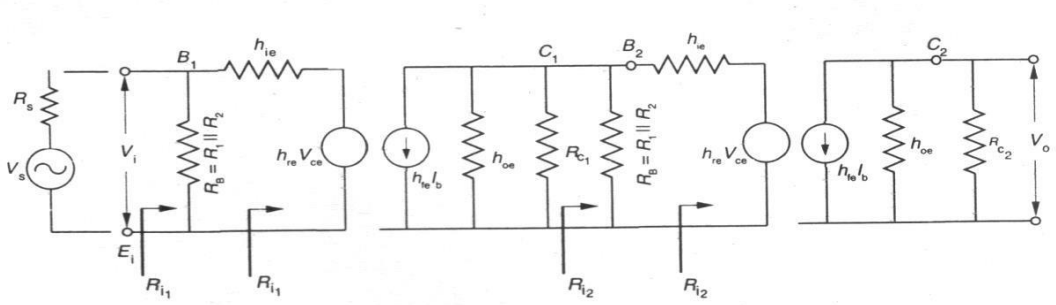


Fig. 5.6 *h*-parameter equivalent circuit for *RC* coupled amplifier

The parallel combination of resistors R_1 and R_2 is replaced by a single stage resistor R_B.

$$R_B = R_1 \| R_2 = R_1R_2/ (R_1 + R_2)$$

For finding the overall gain of the two stage amplifier, we must know the gains of the individual stages.

Current gain (A_{i2}):

$$A_i = - h_{fe} / (1 + h_{oe} R_L)$$

Neglecting h_{oe} as it is very small, $A_i = -h_{fe}$

Input resistance (R_{i2}):

We know that $R_i = h_{ie} + h_{re}A_i R_L$

Hence, $R_i = h_{ie}$ and $R_{i2} = h_{ie}$

Voltage gain (A_{v2}):

We know that $A_v = A_i R_L/ R_i$

$$A_{v2} = - h_{fe} R_{C2} / R_{i2}$$

Current gain (A_{i1}):

$$A_{i1} = -h_{fe}$$

Input resistance (R_{i1}):

$$R_{i1} = h_{ie}$$

Voltage gain (Av1):

$$A_V = A_i R_L / R_{i1}$$

Here $R_L = R_{C1} \parallel R_B \parallel R_{i2}$

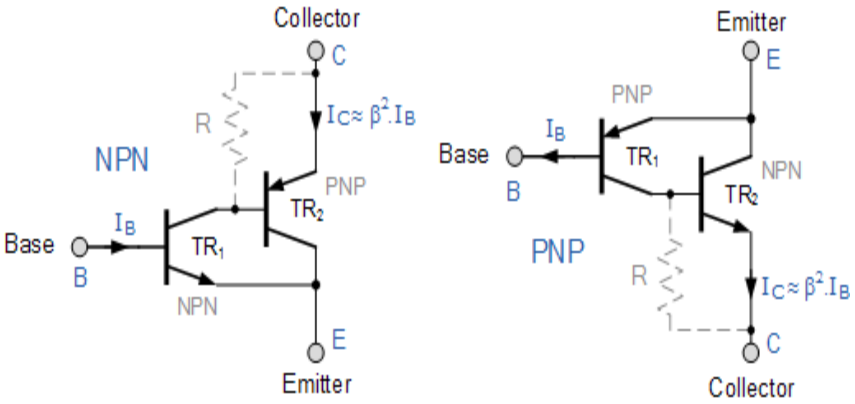
$$A_{V1} = - h_{fe} (R_{C1} \parallel R_B \parallel R_{i2}) / R_{i1}$$

Overall gain (A_v):

$$A_V = A_{V1} \text{ X } A_{V2}$$

A **Darlington Transistor** configuration, also known as a "Darlington pair" or "super-alpha circuit", consist of two NPN or PNP transistors connected together so that the emitter current of the first transistor TR_1 becomes the base current of the second transistor TR_2. Then transistor TR1 is connected as an emitter follower and TR2 as a common emitter amplifier as shown below. Also note that in this Darlington pair configuration, the collector current of the slave or control transistor, TR1 is "in-phase" with that of the master switching transistor TR2.

Basic Darlington Transistor Configuration



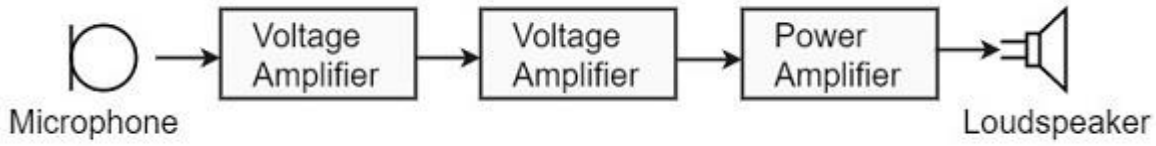
Using the NPN Darlington pair as the example, the collectors of two transistors are connected together, and the emitter of TR_1 drives the base of TR_2. This configuration achieves β multiplication because for a Base current i_b, the collector current is $\beta * i_b$ where the current gain is greater than one, or unity and this is defined as:

But the base current, I_{B2} is equal to transistor TR1 emitter current, I_{E1} as the emitter of TR1 is connected to the base of TR2.

This means that the overall current gain, β is given by the gain of the first transistor multiplied by the gain of the second transistor as the current gains of the two transistors multiply. In other words, a pair of bipolar transistors combined together to make a single Darlington transistor pair can be regarded as a single transistor with a very high value of β and consequently a high input resistance.

POWER AMPLIFIERS

After the audio signal is converted into electrical signal, it has several voltage amplifications done, after which the power amplification of the amplified signal is done just before the loud speaker stage. This is clearly shown in the below figure.



While the voltage amplifier raises the voltage level of the signal, the power amplifier raises the power level of the signal. Besides raising the power level, it can also be said that a power amplifier is a device which converts DC power to AC power and whose action is controlled by the input signal.

The DC power is distributed according to the relation,

$$\text{DC power input} = \text{AC power output} + \text{losses}$$

Power Transistor

For such Power amplification, a normal transistor would not do. A transistor that is manufactured to suit the purpose of power amplification is called as a **Power transistor**.

A Power transistor differs from the other transistors, in the following factors.

- It is larger in size, in order to handle large powers.
- The collector region of the transistor is made large and a heat sink is placed at the collector-base junction in order to minimize heat generated.
- The emitter and base regions of a power transistor are heavily doped.
- Due to the low input resistance, it requires low input power.

Hence there is a lot of difference in voltage amplification and power amplification. So, let us now try to get into the details to understand the differences between a voltage amplifier and a power amplifier.

Difference between Voltage and Power Amplifiers

Let us try to differentiate between voltage and power amplifier.

Voltage Amplifier

The function of a voltage amplifier is to raise the voltage level of the signal. A voltage amplifier is designed to achieve maximum voltage amplification.

The voltage gain of an amplifier is given by

$$Av=\beta(RcRin)Av=\beta(RcRin)$$

The characteristics of a voltage amplifier are as follows −

- The base of the transistor should be thin and hence the value of β should be greater than 100.
- The resistance of the input resistor R_{in} should be low when compared to collector load R_C.
- The collector load R_C should be relatively high. To permit high collector load, the voltage amplifiers are always operated at low collector current.
- The voltage amplifiers are used for small signal voltages.

Power Amplifier

The function of a power amplifier is to raise the power level of input signal. It is required to deliver a large amount of power and has to handle large current.

The characteristics of a power amplifier are as follows −

- The base of transistor is made thicken to handle large currents. The value of β being (β > 100) high.
- The size of the transistor is made larger, in order to dissipate more heat, which is produced during transistor operation.
- Transformer coupling is used for impedance matching.
- Collector resistance is made low.

The Power amplifiers amplify the power level of the signal. This amplification is done in the last stage in audio applications. The applications related to radio frequencies employ radio power amplifiers. But the **operating point** of a transistor, plays a very important role in determining the efficiency of the amplifier. The **main classification** is done based on this mode of operation.

The classification is done based on their frequencies and also based on their mode of operation.

Classification Based on Frequencies:

Power amplifiers are divided into two categories, based on the frequencies they handle. They are as follows.

- **Audio Power Amplifiers** − The audio power amplifiers raise the power level of signals that have audio frequency range (20 Hz to 20 KHz). They are also known as **Small signal power amplifiers**.
- **Radio Power Amplifiers** − Radio Power Amplifiers or tuned power amplifiers raise the power level of signals that have radio frequency range (3 KHz to 300 GHz). They are also known as **large signal power amplifiers**.

Classification Based on Mode of Operation

On the basis of the mode of operation, i.e., the portion of the input cycle during which collector current flows, the power amplifiers may be classified as follows.

- **Class A Power amplifier** − When the collector current flows at all times during the full cycle of signal, the power amplifier is known as **class A power amplifier**.
- **Class B Power amplifier** − When the collector current flows only during the positive half cycle of the input signal, the power amplifier is known as **class B power amplifier**.
- **Class C Power amplifier** − When the collector current flows for less than half cycle of the input signal, the power amplifier is known as **class C power amplifier**.

There forms another amplifier called Class AB amplifier, if we combine the class A and class B amplifiers so as to utilize the advantages of both.

Before going into the details of these amplifiers, let us have a look at the important terms that have to be considered to determine the efficiency of an amplifier.

Terms Considering Performance

The primary objective of a power amplifier is to obtain maximum output power. In order to achieve this, the important factors to be considered are collector efficiency, power dissipation capability and distortion. Let us go through them in detail.

Collector Efficiency

This explains how well an amplifier converts DC power to AC power. When the DC supply is given by the battery but no AC signal input is given, the collector output at such a condition is observed as **collector efficiency**.

The collector efficiency is defined as

$$\eta = \frac{\text{average a.c power output averaged}}{\text{power input to transistor}}$$

For example, if the battery supplies 15W and AC output power is 3W. Then the transistor efficiency will be 20%.

The main aim of a power amplifier is to obtain maximum collector efficiency. Hence the higher the value of collector efficiency, the efficient the amplifier will be.

Power Dissipation Capacity

Every transistor gets heated up during its operation. As a power transistor handles large currents, it gets more heated up. This heat increases the temperature of the transistor, which alters the operating point of the transistor.

So, in order to maintain the operating point stability, the temperature of the transistor has to be kept in permissible limits. For this, the heat produced has to be dissipated. Such a capacity is called as Power dissipation capability.

Power dissipation capability can be defined as the ability of a power transistor to dissipate the heat developed in it. Metal cases called heat sinks are used in order to dissipate the heat produced in power transistors.

Distortion

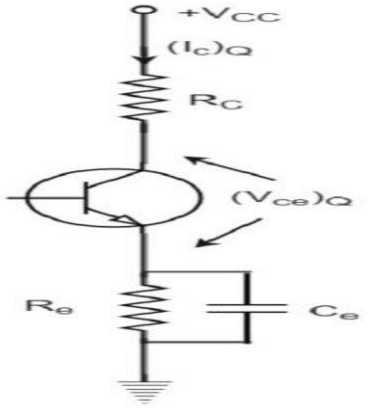
A transistor is a non-linear device. When compared with the input, there occur few variations in the output. In voltage amplifiers, this problem is not pre-dominant as small currents are used. But in power amplifiers, as large currents are in use, the problem of distortion certainly arises.

Distortion is defined as the change of output wave shape from the input wave shape of the amplifier. An amplifier that has lesser distortion, produces a better output and hence considered efficient.

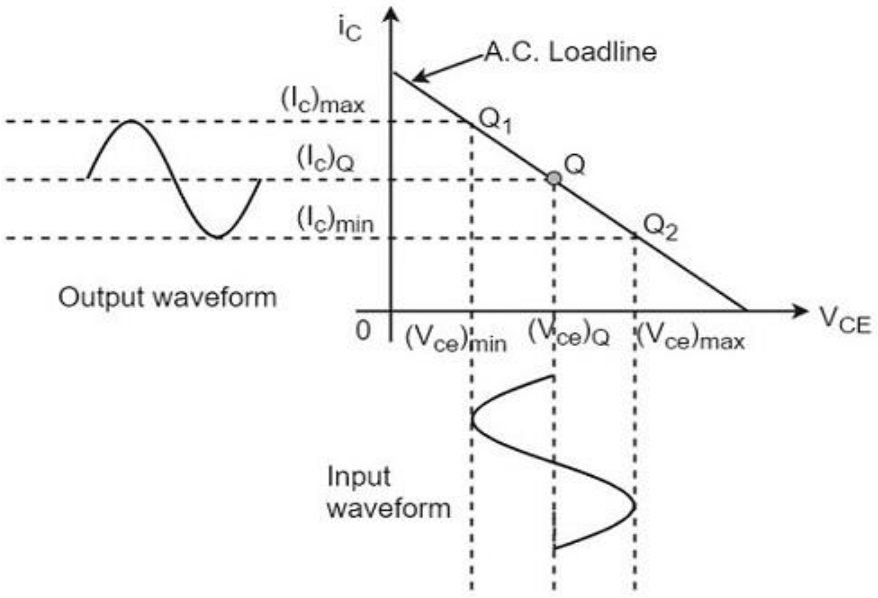
CLASS A POWER AMPLIFIER:

We have already come across the details of transistor biasing, which is very important for the operation of a transistor as an amplifier. Hence to achieve faithful amplification, the biasing of the transistor has to be done such that the amplifier operates over the linear region.

A Class A power amplifier is one in which the output current flows for the entire cycle of the AC input supply. Hence the complete signal present at the input is amplified at the output. The following figure shows the circuit diagram for Class A Power amplifier.



From the above figure, it can be observed that the transformer is present at the collector as a load. The use of transformer permits the impedance matching, resulting in the transference of maximum power to the load e.g. loud speaker.The operating point of this amplifier is present in the linear region. It is so selected that the current flows for the entire ac input cycle. The below figure explains the selection of operating point.



The output characteristics with operating point Q is shown in the figure above. Here $(I_c)_Q$ and $(V_{ce})_Q$ represent no signal collector current and voltage between collector and emitter respectively. When signal is applied, the Q-point shifts to Q_1 and Q_2. The output current increases to $(I_c)_{max}$ and decreases to $(I_c)_{min}$. Similarly, the collector-emitter voltage increases to $(V_{ce})_{max}$ and decreases to $(V_{ce})_{min}$.

D.C. Power drawn from collector battery V_{cc} is given by

Pin=voltage×current=VCC(IC)QPin=voltage×current=VCC(IC)Q

This power is used in the following two parts −

- Power dissipated in the collector load as heat is given by

  PRC=(current)2×resistance=(IC)2QRCPRC=(current)2×resistance=(IC)Q2RC

- Power given to transistor is given by

$$Ptr=Pin−PRC=VCC−(IC)2QRCPtr=Pin−PRC=VCC−(IC)Q2RC$$

When signal is applied, the power given to transistor is used in the following two parts −

- A.C. Power developed across load resistors RC which constitutes the a.c. power output.

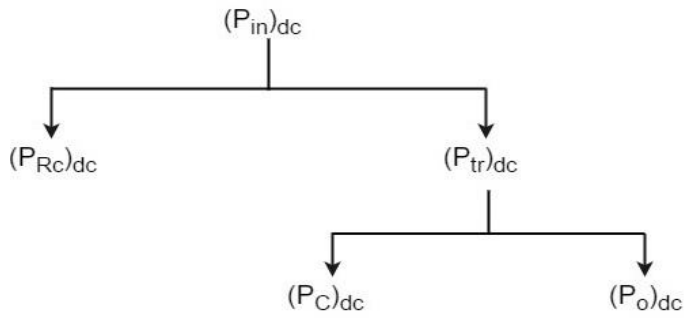
$$(PO)ac=I2RC=V2RC=(Vm2–$$

$$√)21RC=V2m2RC(PO)ac=I2RC=V2RC=(Vm2)21RC=Vm22RC$$

Where **I** is the R.M.S. value of a.c. output current through load, **V** is the R.M.S. value of a.c. voltage, and $\mathbf{V_m}$ is the maximum value of V.

- The D.C. power dissipated by the transistor (collector region) in the form of heat, i.e., $(P_C)_{dc}$

We have represented the whole power flow in the following diagram.



This class A power amplifier can amplify small signals with least distortion and the output will be an exact replica of the input with increased strength.

Let us now try to draw some expressions to represent efficiencies.

Overall Efficiency

The overall efficiency of the amplifier circuit is given by

$$(η)overall=a.cpowerdeliveredtotheloadtotalpowerdeliveredbyd.csupply(η)overall=a.cpowerdelivered totheloadtotalpowerdeliveredbyd.csupply$$
$$=(PO)ac(Pin)dc=(PO)ac(Pin)dc$$

Collector Efficiency

The collector efficiency of the transistor is defined as

$$(η)collector=averagea.cpoweroutputaveraged.cpowerinputtotransistor(η)collector=averagea.cpowero utputaveraged.cpowerinputtotransistor$$
$$=(PO)ac(Ptr)dc=(PO)ac(Ptr)dc$$

Expression for overall efficiency

$$(PO)ac=Vrms×Irms(PO)ac=Vrms×Irms$$
$$=12–√[(Vce)max−(Vce)min2]×12–√[(IC)max−(IC)min2]=12[(Vce)max−(Vce)min2]×12[(IC)max−(IC)min2]$$
$$=[(Vce)max−(Vce)min]×[(IC)max−(IC)min]8=[(Vce)max−(Vce)min]×[(IC)max−(IC)min]8$$

Therefore

$$(\eta)overall=[(Vce)max-(Vce)min]\times[(IC)max-(IC)min]8\times VCC(IC)Q(\eta)overall=[(Vce)max-(Vce)min]\times[(IC)max-(IC)min]8\times VCC(IC)Q$$

Advantages of Class A Amplifiers

The advantages of Class A power amplifier are as follows −

- The current flows for complete input cycle
- It can amplify small signals
- The output is same as input
- No distortion is present

Disadvantages of Class A Amplifiers

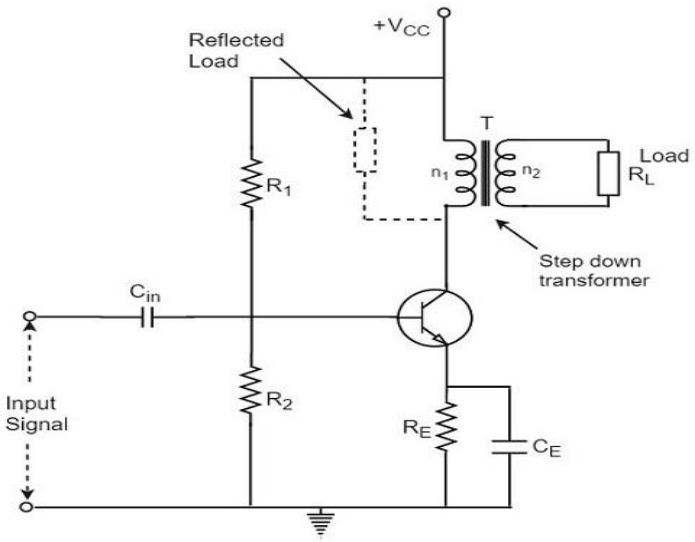
The advantages of Class A power amplifier are as follows −

- Low power output
- Low collector efficiency

TRANSFORMER COUPLED CLASS-A POWER AMPLIFIER

The class A power amplifier as discussed in the previous chapter, is the circuit in which the output current flows for the entire cycle of the AC input supply. We also have learnt about the disadvantages it has such as low output power and efficiency. In order to minimize those effects, the transformer coupled class A power amplifier has been introduced.

The **construction of class A power amplifier** can be understood with the help of below figure. This is similar to the normal amplifier circuit but connected with a transformer in the collector load.

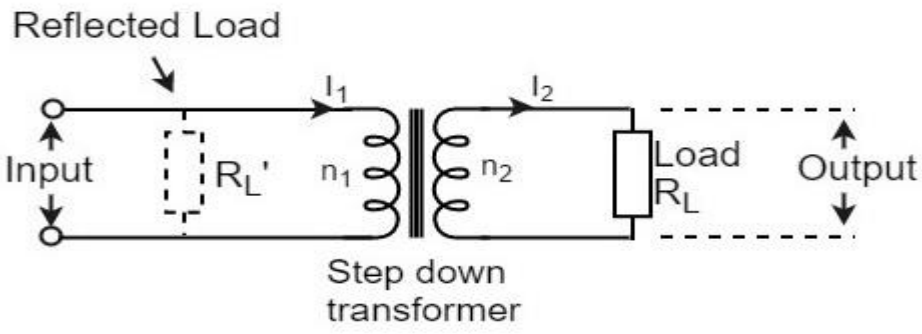


Here R_1 and R_2 provide potential divider arrangement. The resistor Re provides stabilization, C_e is the bypass capacitor and R_e to prevent a.c. voltage. The transformer used here is a step-down transformer. The high impedance primary of the transformer is connected to the high impedance collector circuit. The low impedance secondary is connected to the load (generally loud speaker).

Transformer Action

The transformer used in the collector circuit is for impedance matching. R_L is the load connected in the secondary of a transformer. R_L' is the reflected load in the primary of the transformer.

The number of turns in the primary are n_1 and the secondary are n_2. Let $V_1$and V_2 be the primary and secondary voltages and I_1 and I_2 be the primary and secondary currents respectively. The below figure shows the transformer clearly.



We know that

$$V1V2=n1n2andI1I2=n1n2V1V2=n1n2andI1I2=n1n2$$

Or

$$V1=n1n2V2andI1=n1n2I2V1=n1n2V2andI1=n1n2I2$$

Hence

$$V1I1=(n1n2)2V2I2V1I1=(n1n2)2V2I2$$

But $V_1/I_1 = R_L$' = effective input resistance

And $V_2/I_2 = R_L$ = effective output resistance

Therefore,

$$R'L=(n1n2)2RL=n2RLRL'=(n1n2)2RL=n2RL$$

Where

$$n=numberofturnsinprimarynumberofturnsinsecondary=n1n2n=numberofturnsinprimarynumberofturnsinsecondary=n1n2$$

A power amplifier may be matched by taking proper turn ratio in step down transformer.

Circuit Operation

If the peak value of the collector current due to signal is equal to zero signal collector current, then the maximum a.c. power output is obtained. So, in order to achieve complete amplification, the operating point should lie at the center of the load line.

The operating point obviously varies when the signal is applied. The collector voltage varies in opposite phase to the collector current. The variation of collector voltage appears across the primary of the transformer.

Circuit Analysis

The power loss in the primary is assumed to be negligible, as its resistance is very small.

The input power under dc condition will be

$$(Pin)dc=(Ptr)dc=VCC\times(IC)Q(Pin)dc=(Ptr)dc=VCC\times(IC)Q$$

Under maximum capacity of class A amplifier, voltage swings from $(V_{ce})_{max}$ to zero and current from $(I_c)_{max}$ to zero.

Hence

$$Vrms=12–\sqrt{}[(Vce)max−(Vce)min2]=12–\sqrt{}[(Vce)max2]=2VCC22–\sqrt{}=VCC2–$$
$$\sqrt{}Vrms=12[(Vce)max−(Vce)min2]=12[(Vce)max2]=2VCC22=VCC2$$
$$Irms=12–\sqrt{}[(IC)max−(IC)min2]=12–\sqrt{}[(IC)max2]=2(IC)Q22–\sqrt{}=(IC)Q2–$$
$$\sqrt{}Irms=12[(IC)max−(IC)min2]=12[(IC)max2]=2(IC)Q22=(IC)Q2$$

Therefore,

$$(PO)ac=Vrms\times Irms=VCC2–\sqrt{}\times(IC)Q2–$$
$$\sqrt{}=VCC\times(IC)Q2(PO)ac=Vrms\times Irms=VCC2\times(IC)Q2=VCC\times(IC)Q2$$

Therefore,

$$\text{Collector Efficiency} = (PO)ac(Ptr)dc(PO)ac(Ptr)dc$$

Or,

$$(\eta)collector=VCC\times(IC)Q2\times VCC\times(IC)Q=12(\eta)collector=VCC\times(IC)Q2\times VCC\times(IC)Q=12$$
$$=12\times100=50\%=12\times100=50\%$$

The efficiency of a class A power amplifier is nearly than 30% whereas it has got improved to 50% by using the transformer coupled class A power amplifier.

Advantages

The advantages of transformer coupled class A power amplifier are as follows.

- No loss of signal power in the base or collector resistors.
- Excellent impedance matching is achieved.
- Gain is high.
- DC isolation is provided.

Disadvantages

The disadvantages of transformer coupled class A power amplifier are as follows.

- Low frequency signals are less amplified comparatively.
- Hum noise is introduced by transformers.
- Transformers are bulky and costly.
- Poor frequency response.

Applications

The applications of transformer coupled class A power amplifier are as follows.

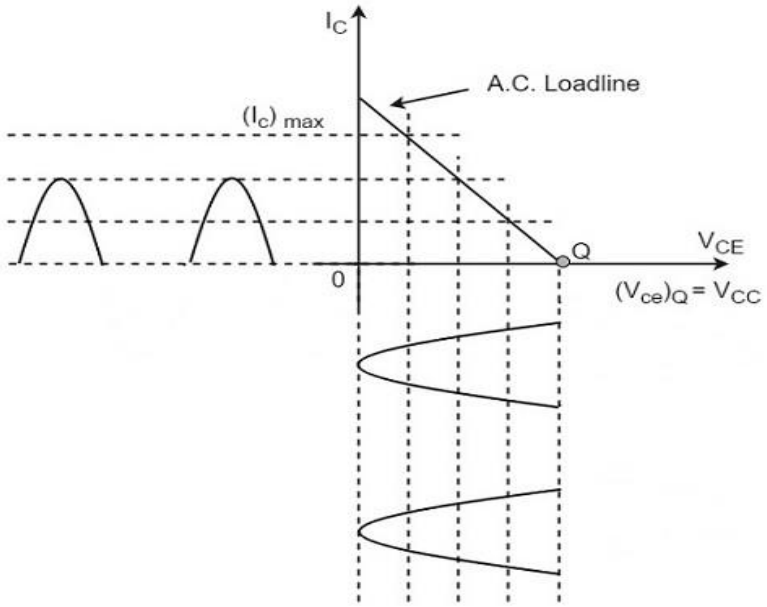
- This circuit is where impedance matching is the main criterion.
- These are used as driver amplifiers and sometimes as output amplifiers.

CLASS –B POWER AMPLIFIER:

Class B Operation

The biasing of the transistor in class B operation is in such a way that at zero signal condition, there will be no collector current. The **operating point** is selected to be at collector cut off voltage. So, when the signal is applied, **only the positive half cycle** is amplified at the output.

The figure below shows the input and output waveforms during class B operation.



When the signal is applied, the circuit is forward biased for the positive half cycle of the input and hence the collector current flows. But during the negative half cycle of the input, the circuit is reverse biased and the collector current will be absent. Hence **only the positive half cycle** is amplified at the output.

As the negative half cycle is completely absent, the signal distortion will be high. Also, when the applied signal increases, the power dissipation will be more. But when compared to class A power amplifier, the output efficiency is increased.

Well, in order to minimize the disadvantages and achieve low distortion, high efficiency and high output power, the push-pull configuration is used in this class B amplifier.

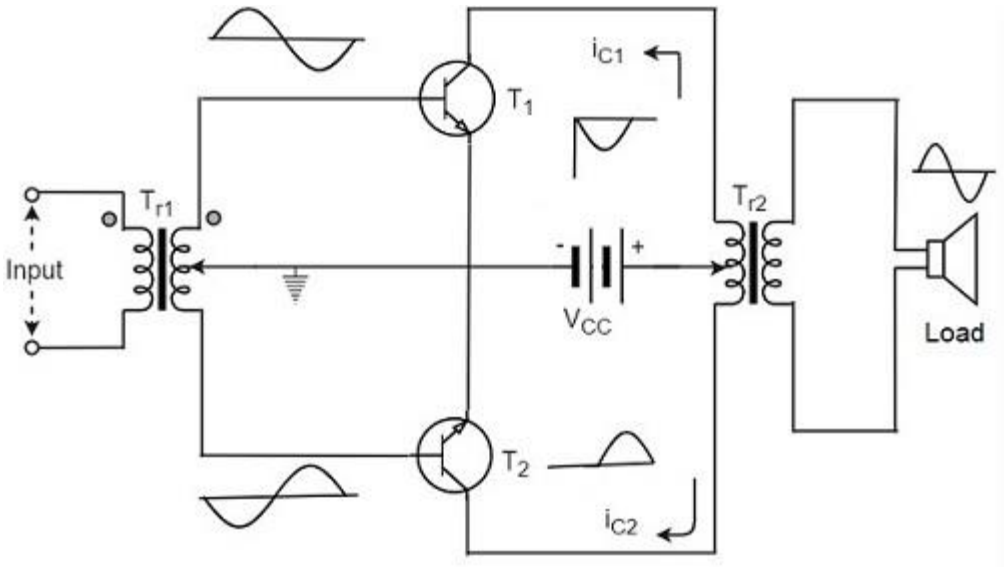
Class B Push-Pull Amplifier

Though the efficiency of class B power amplifier is higher than class A, as only one half cycle of the input is used, the distortion is high. Also, the input power is not completely utilized. In order to compensate these problems, the push-pull configuration is introduced in class B amplifier.

Construction

The circuit of a push-pull class B power amplifier consists of two identical transistors T_1 and T_2 whose bases are connected to the secondary of the center-tapped input transformer T_{r1}. The emitters are shorted and the collectors are given the V_{CC} supply through the primary of the output transformer T_{r2}.

The circuit arrangement of class B push-pull amplifier, is same as that of class A push-pull amplifier except that the transistors are biased at cut off, instead of using the biasing resistors. The figure below gives the detailing of the construction of a push-pull class B power amplifier.

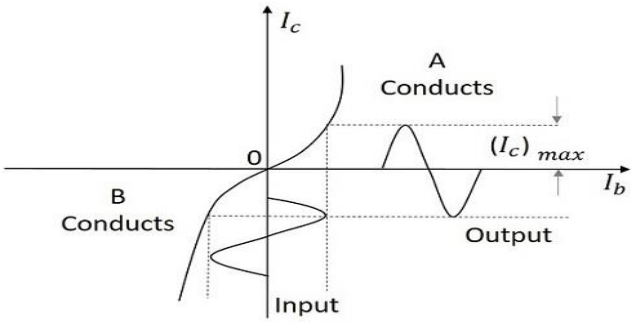


The circuit operation of class B push pull amplifier is detailed below.

Operation

The circuit of class B push-pull amplifier shown in the above figure clears that both the transformers are center-tapped. When no signal is applied at the input, the transistors T_1 and T_2 are in cut off condition and hence no collector currents flow. As no current is drawn from V_{CC}, no power is wasted.

When input signal is given, it is applied to the input transformer T_{r1} which splits the signal into two signals that are 180^o out of phase with each other. These two signals are given to the two identical transistors T_1 and T_2. For the positive half cycle, the base of the transistor T_1 becomes positive and collector current flows. At the same time, the transistor T_2 has negative half cycle, which throws the transistor T_2 into cutoff condition and hence no collector current flows. The waveform is produced as shown in the following figure.



For the next half cycle, the transistor T_1 gets into cut off condition and the transistor T_2 gets into conduction, to contribute the output. Hence for both the cycles, each transistor conducts alternately. The output transformer T_{r3} serves to join the two currents producing an almost undistorted output waveform.

Power Efficiency of Class B Push-Pull Amplifier

The current in each transistor is the average value of half sine loop.

For half sine loop, I_{dc} is given by

$$Idc=(IC)max\pi Idc=(IC)max\pi$$

Therefore,

$$(pin)dc=2\times[(IC)max\pi\times VCC](pin)dc=2\times[(IC)max\pi\times VCC]$$

Here factor 2 is introduced as there are two transistors in push-pull amplifier.

R.M.S. value of collector current = $(IC)max/2–\sqrt{}(IC)max/2$
R.M.S. value of output voltage = $VCC/2–\sqrt{}VCC/2$
Under ideal conditions of maximum power

Therefore,

$$(PO)ac=(IC)max2–\sqrt{}\times VCC2–\sqrt{}=(IC)max\times VCC2(PO)ac=(IC)max2\times VCC2=(IC)max\times VCC2$$

Now overall maximum efficiency

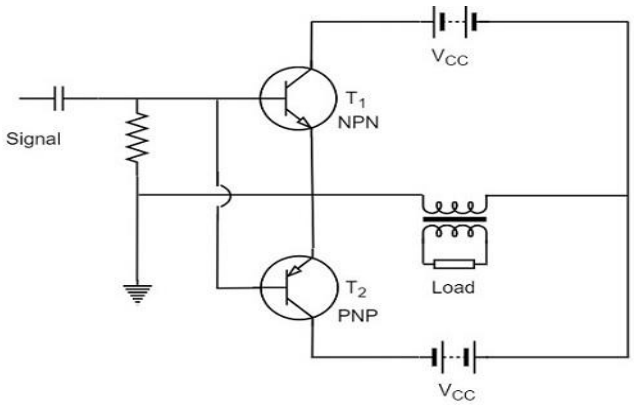
$$\eta overall=(PO)ac(Pin)dc\eta overall=(PO)ac(Pin)dc$$
$$=(IC)max\times VCC2\times\pi2(IC)max\times VCC=(IC)max\times VCC2\times\pi2(IC)max\times VCC$$
$$=\pi4=0.785=78.5\%=\pi4=0.785=78.5\%$$

The collector efficiency would be the same.

Hence the class B push-pull amplifier improves the efficiency than the class A push-pull amplifier.

Complementary Symmetry Push-Pull Class B Amplifier

The push pull amplifier which was just discussed improves efficiency but the usage of center-tapped transformers makes the circuit bulky, heavy and costly. To make the circuit simple and to improve the efficiency, the transistors used can be complemented, as shown in the following circuit diagram.



The above circuit employs a NPN transistor and a PNP transistor connected in push pull configuration. When the input signal is applied, during the positive half cycle of the input signal, the NPN transistor conducts and the PNP transistor cuts off. During the negative half cycle, the NPN transistor cuts off and the PNP transistor conducts. In this way, the NPN transistor amplifies during positive half cycle of the input, while PNP transistor amplifies during negative half cycle of the input. As the transistors are both complement to each other, yet act symmetrically while being connected in push pull configuration of class B, this circuit is termed as **Complementary symmetry push pull class B amplifier**.

Advantages

The advantages of Complementary symmetry push pull class B amplifier are as follows.

- As there is no need of center tapped transformers, the weight and cost are reduced.
- Equal and opposite input signal voltages are not required.

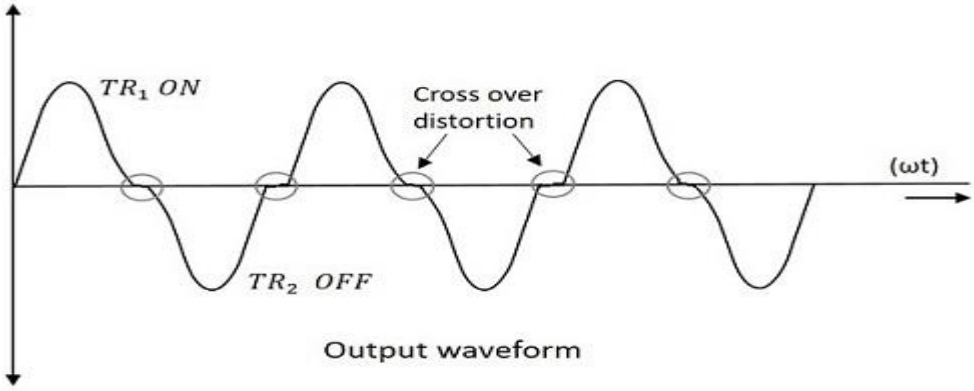
Disadvantages

The disadvantages of Complementary symmetry push pull class B amplifier are as follows.

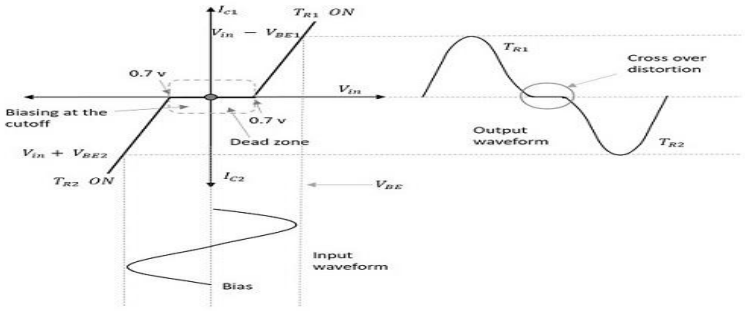
- It is difficult to get a pair of transistors (NPN and PNP) that have similar characteristics.
- We require both positive and negative supply voltages.

Cross-over Distortion

In the push-pull configuration, the two identical transistors get into conduction, one after the other and the output produced will be the combination of both. When the signal changes or crosses over from one transistor to the other at the zero voltage point, it produces an amount of distortion to the output wave shape. For a transistor in order to conduct, the base emitter junction should cross 0.7v, the cut off voltage. The time taken for a transistor to get ON from OFF or to get OFF from ON state is called the **transition period**. At the zero voltage point, the transition period of switching over the transistors from one to the other, has its effect which leads to the instances where both the transistors are OFF at a time. Such instances can be called as **Flat spot** or **Dead band** on the output wave shape.



The above figure clearly shows the cross over distortion which is prominent in the output waveform. This is the main disadvantage. This cross over distortion effect also reduces the overall peak to peak value of the output waveform which in turn reduces the maximum power output. This can be more clearly understood through the non-linear characteristic of the waveform as shown below.

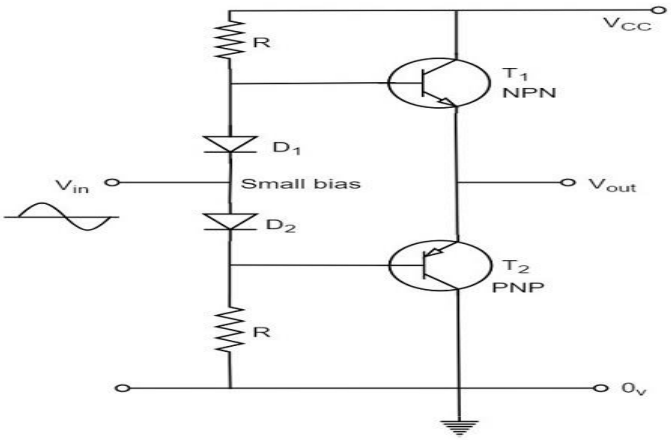


It is understood that this cross-over distortion is less pronounced for large input signals, where as it causes severe disturbance for small input signals. This cross over distortion can be eliminated if the conduction of the amplifier is more than one half cycle, so that both the transistors won't be OFF at the same time. This idea leads to the invention of class AB amplifier, which is the combination of both class A and class B amplifiers, as discussed below.

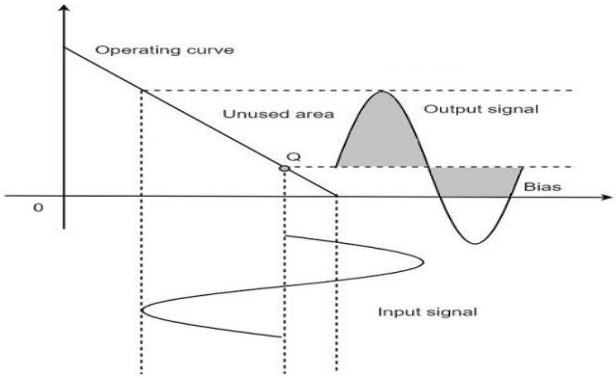
Class AB Power Amplifier

As the name implies, class AB is a combination of class A and class B type of amplifiers. As class A has the problem of low efficiency and class B has distortion problem, this class AB is emerged to eliminate these two problems, by utilizing the advantages of both the classes.

The cross over distortion is the problem that occurs when both the transistors are OFF at the same instant, during the transition period. In order to eliminate this, the condition has to be chosen for more than one half cycle. Hence, the other transistor gets into conduction, before the operating transistor switches to cut off state. This is achieved only by using class AB configuration, as shown in the following circuit diagram.



Therefore, in class AB amplifier design, each of the push-pull transistors is conducting for slightly more than the half cycle of conduction in class B, but much less than the full cycle of conduction of class A. The conduction angle of class AB amplifier is somewhere between 180^o to 360^o depending upon the operating point selected. This is understood with the help of below figure.

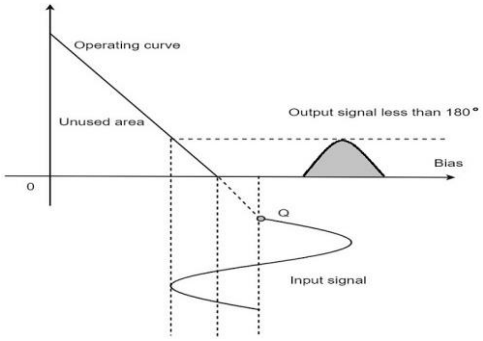


The small bias voltage given using diodes D_1 and D_2, as shown in the above figure, helps the operating point to be above the cutoff point. Hence the output waveform of class AB results as seen in the above figure. The crossover distortion created by class B is overcome by this class AB, as well the inefficiencies of class A and B don't affect the circuit.

So, the class AB is a good compromise between class A and class B in terms of efficiency and linearity having the efficiency reaching about 50% to 60%. The class A, B and AB amplifiers are called as **linear amplifiers** because the output signal amplitude and phase are linearly related to the input signal amplitude and phase.

Class C Power Amplifier

When the collector current flows for less than half cycle of the input signal, the power amplifier is known as **class C power amplifier**. The efficiency of class C amplifier is high while linearity is poor. The conduction angle for class C is less than 180^o. It is generally around 90^o, which means the transistor remains idle for more than half of the input signal. So, the output current will be delivered for less time compared to the application of input signal. The following figure shows the operating point and output of a class C amplifier.



This kind of biasing gives a much improved efficiency of around 80% to the amplifier, but introduces heavy distortion in the output signal. Using the class C amplifier, the pulses produced at its output can be converted to complete sine wave of a particular frequency by using LC circuits in its collector circuit.

MODULE-IV
FEEDBACK AMPLIFIERS

Concepts of feedback: Classification of feedback amplifiers, general characteristics of Negative

feedback amplifiers, effect of feedback on amplifier characteristics, voltage series, voltage shunt, current series and current shunt feedback configurations, simple problems; Oscillators: Condition for Oscillations, RC type Oscillators RC phase shift and Wien-bridge Oscillators, LC type Oscillators, generalized analysis of LC Oscillators, Hartley and Colpitts oscillators.

INTRODUCTION TO FEEDBACK AMPLIFIERS

Feedback is a common phenomenon in nature. It plays an important role in electronics & control systems. Feedback is a process whereby a portion of the output signal of the amplifier is feedback to the input of the amplifier. The feedback signal can be either a voltage or a current, being applied in series or shunt respectively with the input signal.

The path over which the feedback is applied is the feedback loop. There are two types of feedback used in electronic circuits. (i) If the feedback voltage or current is in phase with the input signal and adds to its magnitude, the feedback is called positive or regenerative feedback.(ii) If the feedback voltage or current is opposite in phase to the input signal and opposes it , the feedback is called negative or regenerative feedback.

CLASSIFICATION OF AMPLIFIERS:

Before analyzing the concept of feedback, it is useful to classify amplifiers based on the magnitudes of the input & output impedances of an amplifier relative to the sources & load impedances respectively as (i) voltage (ii) current (iii) Tran conductance (iv) Tran resistance amplifiers.

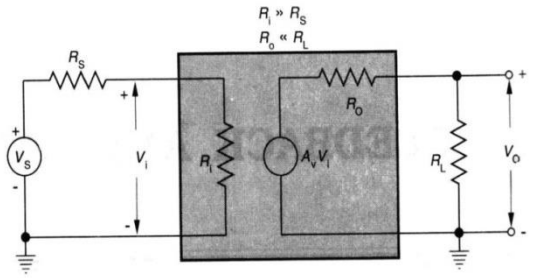


Fig. 4 Thevenin's equivalent circuit of a voltage amplifier

VOLTAGE AMPLIFIER:

The above figure shows a Thevenin's equivalent circuit of an amplifier. If the input resistance of the amplifier Ri is large compared with the source resistance Rs, then Vi = Vs. If the external load RL is large compared with the output resistance R0 of the amplifier, then V0 = AV VS .This type

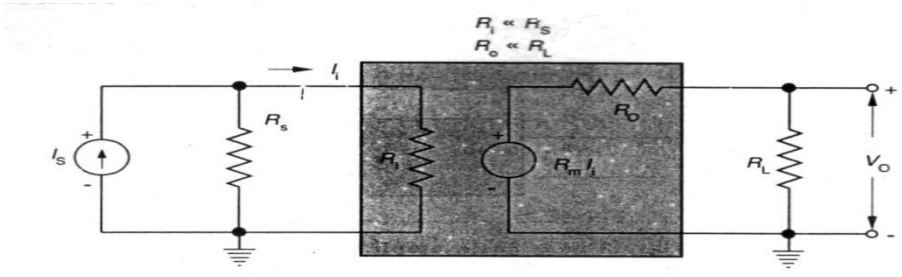


Fig. 7 Equivalent circuit of a transresistance amplifier

of amplifier provides a voltage output proportional to the input voltage & the proportionality factor doesn't depend on the magnitudes of the source and load resistances. Hence, this amplifier is known as voltage amplifier. An ideal voltage amplifier must have infinite resistance Ri and zero output resistance.

CURRENT AMPLIFIER:

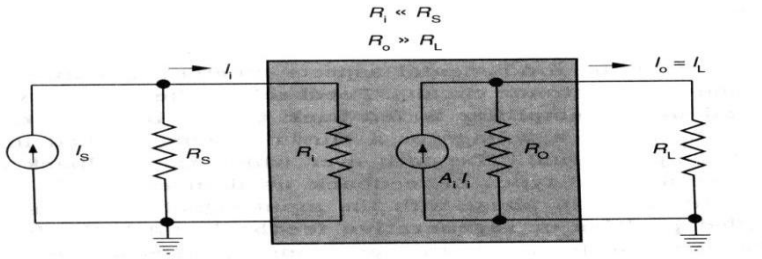


Fig. 5 Norton's equivalent circuit of a current amplifier

Above figure shows a Norton's equivalent circuit of a current amplifier. If the input resistance of the amplifier Ri is very low compared to the source resistance RS, then Ii = IS. If the output resistance of the amplifier R0 is very large compared to external load RL, then IL = AiIi = Ai IS. This amplifier provides an output current proportional to the signal current and the proportionally is dependent of the source and load resistance. Hence, this amplifier is called a current amplifier. An ideal current amplifier must have zero input resistance & infinite output resistance.

TRANSCONDUCTANCE AMPLIFIER:

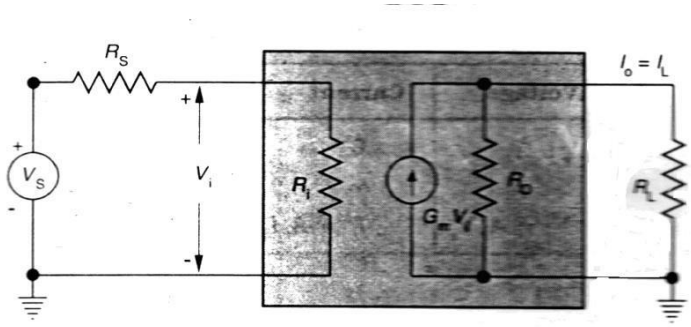


Fig. 6 Equivalent circuit of a transconductance amplifier

The above figure shows the equivalent circuit of a transconductance amplifier. In this circuit, the output current I0 is proportional to the signal voltage VS and the proportionality factor is independent of the magnitudes of source and load resistances. An ideal transconductance amplifier must have an infinite resistance Ri & infinite output resistance R0.

TRANSRESISTANCE AMPLIFIER:

Figure above shows the equivalent circuit of a transconductance amplifier. Here, the output voltage V0 is proportional to the signal current IS and the proportionality factor is independent of magnitudes of source and loads resistances. If RS >>Ri , then Ii = IS , Output voltage V0 = RmIS

An ideal transconductance amplifier must have zero input resistance and zero output resistance.

THE FEEDBACK CONCEPT:

In each of the above discussed amplifiers, we can sample the output voltage or current by means of a suitable sampling network & this sampled portion is feedback to the input through a feedback network as shown below.

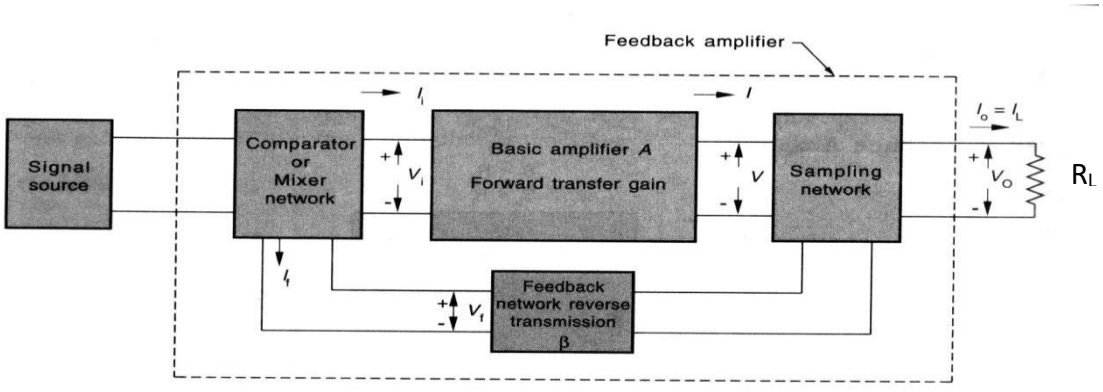


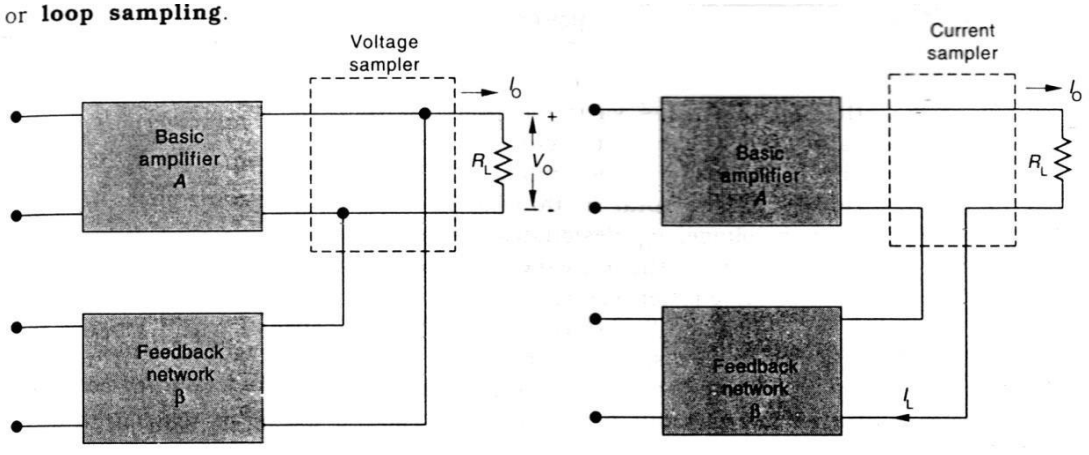
Fig. 1 Block diagram of a basic amplifier with feedback connection

All the input of the amplifier, the feedback signal is combined with the source signal through a unit called mixer. The signal source shown in the above figure can be either a voltage source VS or a current source. The feedback connection has three networks.

1. Sampling network
2. Feedback network
3. Mixer network

SAMPLING NETWORK:

There are two ways to sample the output, depending on the required feedback parameter. The output voltage is sampled by connecting the feedback network in shunt with the output. This is called as voltage sampling.



(a) Voltage or node sampling

Fig. 2

(b) Current or loop sampling

FEEDBACK NETWORK:

This is usually a passive two-port network consisting of resistors, capacitors and inductors. In case of a voltage shunt feedback, it provides a fraction of the output voltage as feedback signal Vf to the input of the mixer.

MIXER:

There are two ways of mixing the feedback signal with the input signal with the input signal as shown in figure . below.

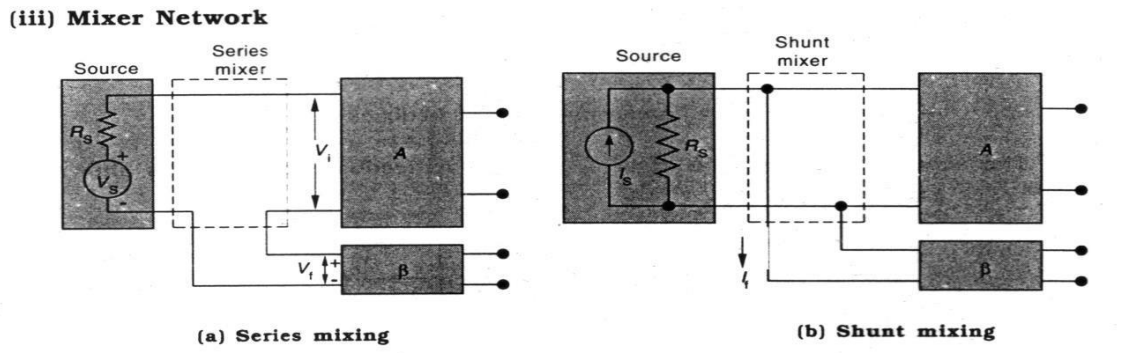


Fig. 3 'eedback connections of the input of a basic amplifier

When the feedback voltage is applied in series with the input voltage through the feedback network as shown in figure 6.7 (a) above, it is called series mixing. Otherwise, when the feedback voltage is applied in parallel to the input of the amplifier as shown in figure (b) above, it is called shunt feedback.

GAIN OR TRANSFER RATIO:

The ratio of the output signal to the input signal of the basic amplifier is represented by the symbol A , with proper suffix representing the different quantities.

TYPES OF FEEDBACK:

Feedback amplifiers can be classified as positive or negative feedback depending on how the feedback signal gets added to the incoming signal. If the feedback signal is of the same sign as the incoming signal, they get added & this is called as positive feedback. On the other hand, if the feedback signal is in phase inverse with the incoming signal, they get subtracted from each other; it will be called as negative feedback amplifier. Positive feedback is employed in oscillators whereas negative feedback is used in amplifiers.

FEATURE OF NEGATIVE FEEDBACK AMPLIFIERS:

- Overall gain is reduced
- Bandwidth is improved
- Distortion is reduced
- Stability is improved
- Noise is reduced

ANALYSIS OF FEEDBACK AMPLIFIER:

The analysis of the feedback amplifier can be carried out by replacing each active element (BJT, FET) by its small signal model and by writing Kirchoff's loop or nodal equations. Consider the schematic representation of the feedback amplifier as shown below.

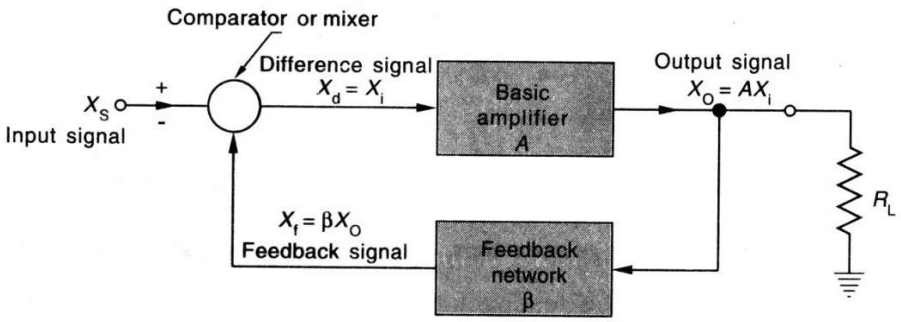
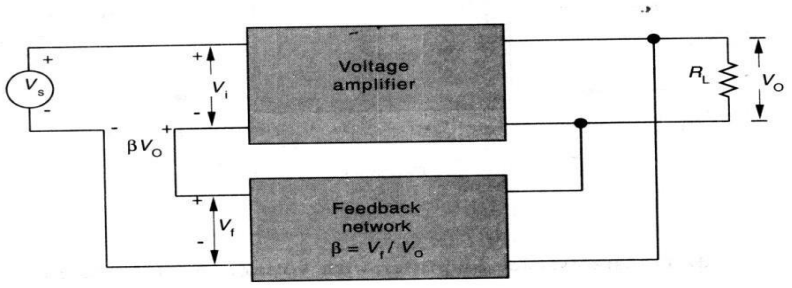
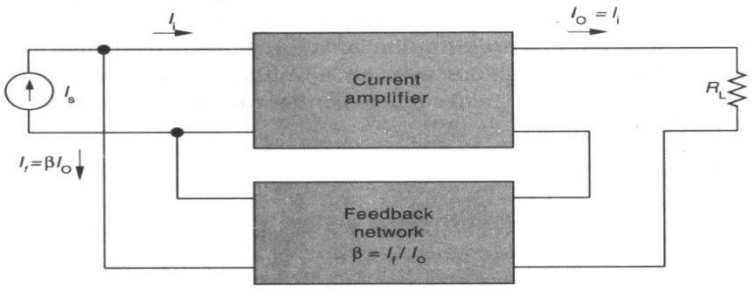


Fig. 4 Schematic representation of a single-loop feedback amplifier

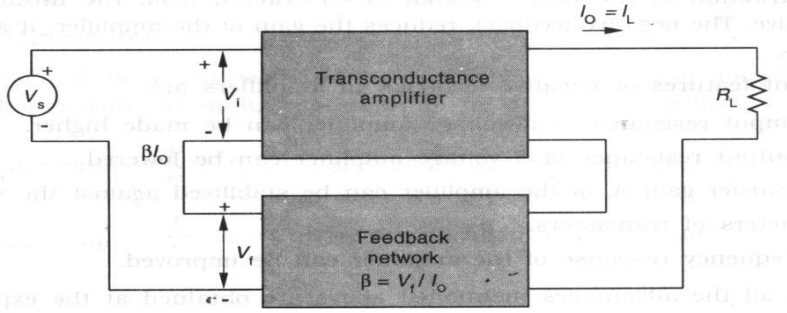


(a) Voltage amplifier with voltage-series feedback

Fig. 5 Types of amplifiers with negative feedback



(c) Current amplifier with current-shunt feedback



(b) Transconductance amplifier with current-series feedback

The four basic types of feedback are:

- Voltage –Series feedback
- Current – Series feedback
- Current – Shunt feedback
- Voltage – Shunt feedback

GAIN WITH FEEDBACK:

Consider the schematic representation of negative feedback amplifier as shown in fig.6.8.The source resistance RS to be part of the amplifier & transfer gain A (AV,Ai ,Gm ,Rm) includes the effect of the loading of the □ network upon the amplifier.The input signal XS, the output signal X0, the feedback signal Xf and the difference signal Xd , each represents either a voltage or a current and also the ratios A and □ as summarized below.

The gain, A = X0 / XS (1)

The output of the mixer,

Xd = Xs + (-Xf) = Xi (2)

The feedback ratio , □ = Xf / X0 (3)

The overall gain (including the feedback)

Af = X0 / XS (4)

From equation (2), XS = Xi + Xf Af = X0 / (Xi + Xf)

Dividing both numerator and denominator by Xi and simplifying, we get Af = A / (1 + □A) (5)

Equation (5) indicates that the overall gain Af is less the open loop gain. The denominator term (1 + □A) in equation (5) is called the loop gain. The forward path consists only of the basic amplifier, whereas the feedback is in the return path.

GAIN STABILITY:

Gain of an amplifier depends on the factors such as temperature, operating point aging etc. It can be shown that the negative feedback tends to stabilize the gain. The ratio of fractional change in amplification with feedback to the fractional change in without feedback is called the sensitivity of the gain

REDUCTION IN FREQUENCY DISTORTION:

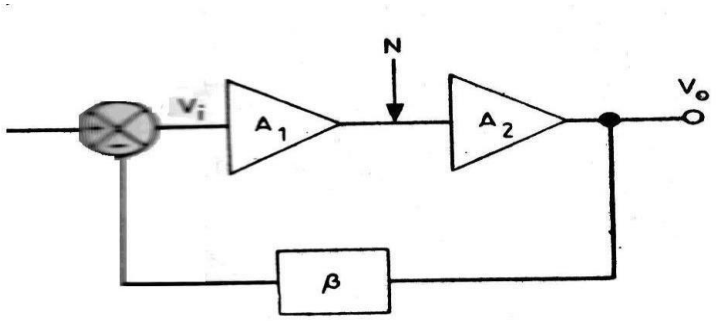
If the feedback network is purely resistive, the overall gain is then not a function of frequency even though the basic amplifier gain is frequency dependent. Under such conditions a substantial reduction in frequency & phase distortion is obtained.

NONLINEAR DISTORTION:

Negative feedback tends to reduce the amount of noise and non-linear distortion. Suppose that a large amplitude signal is applied to an amplifier, so that the operation of the device extends slightly beyond its range of linear operation and as a consequence the output signal is distorted. Negative feedback is now introduced and the input signal is increased by the same amount by which the gain is reduced, so that the output signal amplitude remains the same. Assume that the second harmonic component, in the absence of feedback is B2. Because of feedback, a component B2f actually appears in the output. To find the relationship that exists between B2f& B2, it is noted that the output will contain the term $-A\beta B2f$, which arises from the component $-\beta B2f$ that is feedback to the input. Thus the output contains two terms: B2, generated in the transistor and $-A\beta B2f$, which represents the effect of the feedback. Thus, it is seen that, the negative feedback tends to reduce the second harmonic distortion by the factor $(1+\beta A)$.

NOISE:

Noise or hum components introduced into an amplifier inside the feedback loop are reduced by the feedback loop. Suppose there are two stages of amplifier with gains A1 & A 2 and noise or hum pick-up is introduced after the amplifier with gain A1 as shown in the fig. below



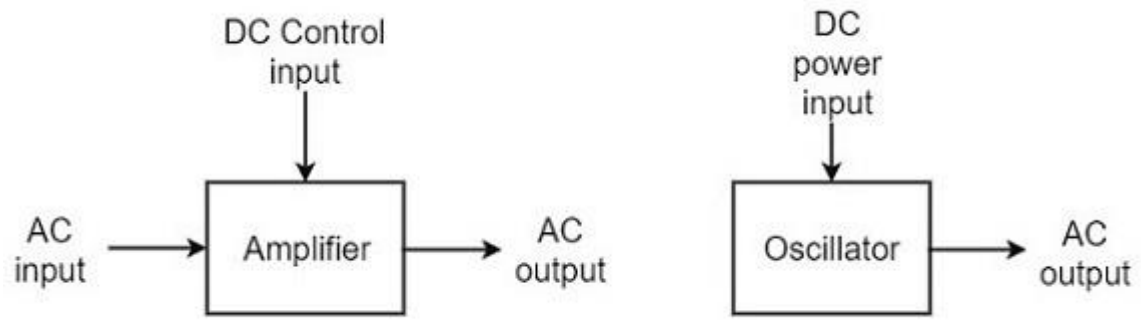
The overall gain of the two stage amplifier is reduced by the factor $1 + A1A2\beta$. In addition the noise output is reduced by the additional factor A1 which is the gain that precedes the introduction of noise. In a single stage amplifier, noise will be reduced by the factor $1/(1 + A\beta)$ just like distortion. But if signal-to-noise ratio has to improve, we have to increase the signal level at the input by the factor $(1 + A\beta)$ to bring back the signal level to the same value as obtained without feedback. If we can assume that noise does not further increase when we increase the signal input, we can conclude that noise is reduced by the factor $1/(1+A\beta)$ due to feedback while the signal level is maintained constant.

OSCILLATORS:

An **oscillator** generates output without any ac input signal. An electronic oscillator is a circuit which converts dc energy into ac at a very high frequency. An amplifier with a positive feedback can be understood as an oscillator.

Amplifier vs. Oscillator

An **amplifier** increases the signal strength of the input signal applied, whereas an **oscillator** generates a signal without that input signal, but it requires dc for its operation. This is the main difference between an amplifier and an oscillator. Take a look at the following illustration. It clearly shows how an amplifier takes energy from d.c. power source and converts it into a.c. energy at signal frequency. An oscillator produces an oscillating a.c. signal on its own.



The frequency, waveform, and magnitude of a.c. power generated by an amplifier, is controlled by the a.c. signal voltage applied at the input, whereas those for an oscillator are controlled by the components in the circuit itself, which means no external controlling voltage is required.

Alternator vs. Oscillator

An **alternator** is a mechanical device that produces sinusoidal waves without any input. This a.c. generating machine is used to generate frequencies up to 1000Hz. The output frequency depends on the number of poles and the speed of rotation of the armature.

The following points highlight the differences between an alternator and an oscillator −

- An alternator converts mechanical energy to a.c. energy, whereas the oscillator converts d.c. energy into a.c. energy.
- An oscillator can produce higher frequencies of several MHz whereas an alternator cannot.
- An alternator has rotating parts, whereas an electronic oscillator doesn't.
- It is easy to change the frequency of oscillations in an oscillator than in an alternator.

Oscillators can also be considered as opposite to rectifiers that convert a.c. to d.c. as these convert d.c. to a.c. You can get a detailed description on rectifiers in our Electronic Circuits tutorial.

Classification of Oscillators

Electronic oscillators are classified mainly into the following two categories −

- **Sinusoidal Oscillators** − The oscillators that produce an output having a sine waveform are called **sinusoidal** or **harmonic oscillators**. Such oscillators can provide output at frequencies ranging from 20 Hz to 1 GHz.
- **Non-sinusoidal Oscillators** − The oscillators that produce an output having a square, rectangular or saw-tooth waveform are called **non-sinusoidal** or **relaxation oscillators**. Such oscillators can provide output at frequencies ranging from 0 Hz to 20 MHz.

- **Sinusoidal Oscillators**

Sinusoidal oscillators can be classified in the following categories −

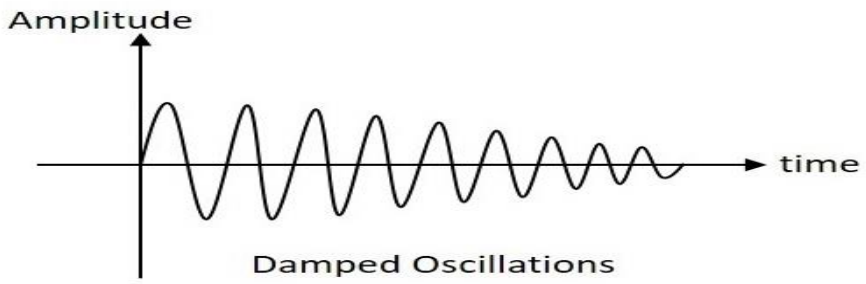
- **Tuned Circuit Oscillators** − These oscillators use a tuned-circuit consisting of inductors (L) and capacitors (C) and are used to generate high-frequency signals. Thus they are also known as radio frequency R.F. oscillators. Such oscillators are Hartley, Colpitts, Clapp-oscillators etc.
- **RC Oscillators** − There oscillators use resistors and capacitors and are used to generate low or audio-frequency signals. Thus they are also known as audio-frequency (A.F.) oscillators. Such oscillators are Phase –shift and Wein-bridge oscillators.
- **Crystal Oscillators** − These oscillators use quartz crystals and are used to generate highly stabilized output signal with frequencies up to 10 MHz. The Piezo oscillator is an example of a crystal oscillator.
- **Negative-resistance Oscillator** − These oscillators use negative-resistance characteristic of the devices such as tunnel devices. A tuned diode oscillator is an example of a negative-resistance oscillator.

Nature of Sinusoidal Oscillations

The nature of oscillations in a sinusoidal wave are generally of two types. They are damped and undamped oscillations.

Damped Oscillations

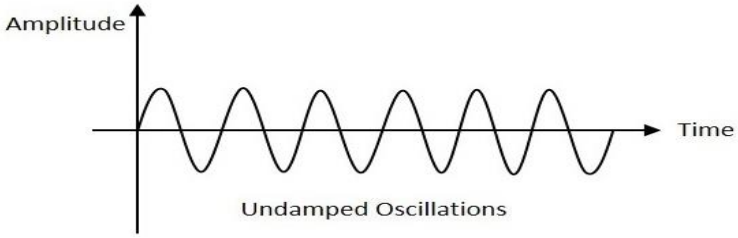
The electrical oscillations whose amplitude goes on decreasing with time are called as **Damped Oscillations**. The frequency of the damped oscillations may remain constant depending upon the circuit parameters.



Damped oscillations are generally produced by the oscillatory circuits that produce power losses and doesn't compensate if required.

Undamped Oscillations

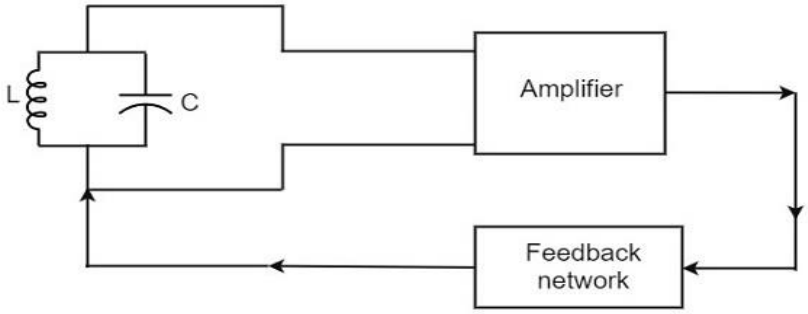
The electrical oscillations whose amplitude remains constant with time are called as **Undamped Oscillations**. The frequency of the Undamped oscillations remains constant.



Undamped oscillations are generally produced by the oscillatory circuits that produce no power losses and follow compensation techniques if any power losses occur. An Oscillator circuit is a complete set of all the parts of circuit which helps to produce the oscillations. These oscillations should sustain and should be Undamped as just discussed before. Let us try to analyze a practical Oscillator circuit to have a better understanding on how an Oscillator circuit works.

Practical Oscillator Circuit

A Practical Oscillator circuit consists of a tank circuit, a transistor amplifier, and a feedback circuit. The following circuit diagram shows the arrangement of a practical oscillator.



Let us now discuss the parts of this practical oscillator circuit.

- **Tank Circuit** − The tank circuit consists of an inductance L connected in parallel with capacitor **C**. The values of these two components determine the frequency of the oscillator circuit and hence this is called as **Frequency determining circuit**.
- **Transistor Amplifier** − The output of the tank circuit is connected to the amplifier circuit so that the oscillations produced by the tank circuit are amplified here. Hence the output of these oscillations are increased by the amplifier.
- **Feedback Circuit** − The function of feedback circuit is to transfer a part of the output energy to LC circuit in proper phase. This feedback is positive in oscillators while negative in amplifiers.

Frequency Stability of an Oscillator

The frequency stability of an oscillator is a measure of its ability to maintain a constant frequency, over a long time interval. When operated over a longer period of time, the oscillator frequency may have a drift from the previously set value either by increasing or by decreasing.

The change in oscillator frequency may arise due to the following factors −

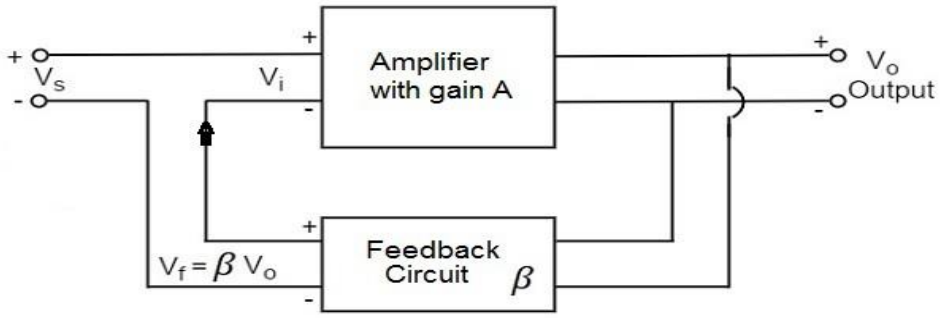
- Operating point of the active device such as BJT or FET used should lie in the linear region of the amplifier. Its deviation will affect the oscillator frequency.
- The temperature dependency of the performance of circuit components affect the oscillator frequency.
- The changes in d.c. supply voltage applied to the active device, shift the oscillator frequency. This can be avoided if a regulated power supply is used.
- A change in output load may cause a change in the Q-factor of the tank circuit, thereby causing a change in oscillator output frequency.
- The presence of inter element capacitances and stray capacitances affect the oscillator output frequency and thus frequency stability.

The Barkhausen Criterion

With the knowledge we have till now, we understood that a practical oscillator circuit consists of a tank circuit, a transistor amplifier circuit and a feedback circuit. so, let us now try to brush up the concept of feedback amplifiers, to derive the gain of the feedback amplifiers.

Principle of Feedback Amplifier

A feedback amplifier generally consists of two parts. They are the **amplifier** and the **feedback circuit**. The feedback circuit usually consists of resistors. The concept of feedback amplifier can be understood from the following figure below.



From the above figure, the gain of the amplifier is represented as A. The gain of the amplifier is the ratio of output voltage Vo to the input voltage V_i. The feedback network extracts a voltage $V_f = \beta V_o$ from the output V_o of the amplifier.

This voltage is added for positive feedback and subtracted for negative feedback, from the signal voltage V_s.

So, for a positive feedback,

$$V_i = V_s + V_f = V_s + \beta V_o$$

The quantity $\beta = V_f/V_o$ is called as feedback ratio or feedback fraction.

The output V_o must be equal to the input voltage $(V_s + \beta V_o)$ multiplied by the gain A of the amplifier.

Hence,

$$(Vs+\beta Vo)A=Vo(Vs+\beta Vo)A=Vo \quad \textbf{Or}$$
$$AVs+A\beta Vo=VoAVs+A\beta Vo=Vo \quad \textbf{Or}$$
$$AVs=Vo(1-A\beta)AVs=Vo(1-A\beta)$$
$$\text{Therefore , } VoVs=A1-A\beta VoVs=A1-A\beta$$

Let A_f be the overall gain (gain with the feedback) of the amplifier. This is defined as the ratio of output voltage V_o to the applied signal voltage V_s, i.e.,

$$Af=OutputVoltageInputSignal$$
$$Voltage=VoVsAf=OutputVoltageInputSignalVoltage=VoVs$$

from the above two equations, we can understand that, the equation of gain of the feedback amplifier with positive feedback is given by

$$Af=A1-A\beta Af=A1-A\beta$$

Where **Aβ** is the **feedback factor** or the **loop gain**.

If $A\beta = 1$, $A_f = \infty$. Thus the gain becomes infinity, i.e., there is output without any input. In another words, the amplifier works as an Oscillator.

The condition $A\beta = 1$ is called as **Barkhausen Criterion of oscillations**. This is a very important factor to be always kept in mind, in the concept of Oscillators.

Tuned circuit oscillators are the circuits that produce oscillations with the help of tuning circuits. The tuning circuits onsists of an inductance L and a capacitor C. These are also known as **LC oscillators, resonant circuit oscillators** or **tank circuit oscillators**.

The tuned circuit oscillators are used to produce an output with frequencies ranging from 1 MHz to 500 MHz Hence these are also known as **R.F. Oscillators**. A BJT or a FET is used as an amplifier with tuned circuit oscillators. With an amplifier and an LC tank circuit, we can feedback a signal with right amplitude and phase to maintain oscillations.

Types of Tuned Circuit Oscillators

Most of the oscillators used in radio transmitters and receivers are of LC oscillators type. Depending upon the way the feedback is used in the circuit, the LC oscillators are divided as the following types.

- **Tuned-collector or Armstrong Oscillator** − It uses inductive feedback from the collector of a transistor to the base. The LC circuit is in the collector circuit of the transistor.
- **Tuned base Oscillator** − It uses inductive feedback. But the LC circuit is in the base circuit.
- **Hartley Oscillator** − It uses inductive feedback.
- **Colpitts Oscillator** − It uses capacitive feedback.
- **Clapp Oscillator** − It uses capacitive feedback.

Hartley Oscillator:

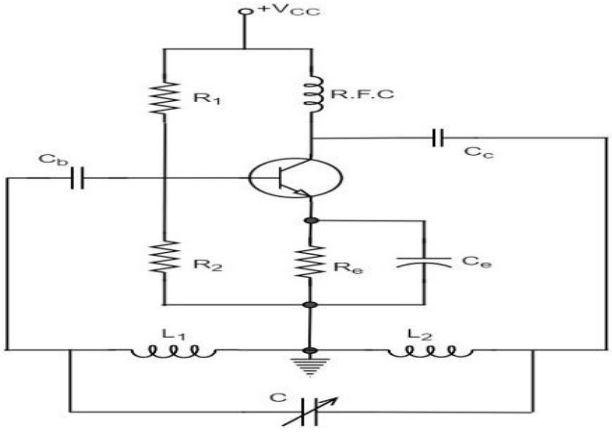
A very popular **local oscillator** circuit that is mostly used in **radio receivers** is the **Hartley Oscillator** circuit. The constructional details and operation of a Hartley oscillator are as discussed below.

Construction

In the circuit diagram of a Hartley oscillator shown below, the resistors R_1, $R_2$and R_e provide necessary bias condition for the circuit. The capacitor C_e provides a.c. ground thereby providing any signal degeneration. This also provides temperature stabilization. The capacitors C_c and C_b are employed to block d.c. and to provide an a.c. path. The radio frequency choke (R.F.C) offers very high impedance to high frequency currents which means it shorts for d.c. and opens for a.c. Hence it provides d.c. load for collector and keeps a.c. currents out of d.c. supply source

Tank Circuit

The frequency determining network is a parallel resonant circuit which consists of the inductors L_1 and L_2 along with a variable capacitor C. The junction of $L_1$and L_2 are earthed. The coil L_1 has its one end connected to base via C_c and the other to emitter via C_e. So, L_2 is in the output circuit. Both the coils L_1 and L_2 are inductively coupled and together form an **Auto-transformer**. The following circuit diagram shows the arrangement of a Hartley oscillator. The tank circuit is **shunt fed** in this circuit. It can also be a **series-fed**.



Operation

When the collector supply is given, a transient current is produced in the oscillatory or tank circuit. The oscillatory current in the tank circuit produces a.c. voltage across L_1. The **auto-transformer** made by the inductive coupling of L_1 and L_2 helps in determining the frequency and establishes the feedback. As the CE configured transistor provides 180^o phase shift, another 180^o phase shift is provided by the transformer, which makes 360^o phase shift between the input and output voltages. This makes the feedback positive which is essential for the condition of oscillations. When the **loop gain |βA| of the amplifier is greater than one**, oscillations are sustained in the circuit.

Frequency

The equation for **frequency of Hartley oscillator** is given as

$$f=12\pi LTC----\sqrt{}f=12\pi LTC$$
$$LT=L1+L2+2MLT=L1+L2+2M$$

Here, $\mathbf{L_T}$ is the total cumulatively coupled inductance; $\mathbf{L_1}$ and $\mathbf{L_2}$ represent inductances of 1^{st} and 2^{nd} coils; and **M** represents mutual inductance. **Mutual inductance** is calculated when two windings are considered.

Advantages

The advantages of Hartley oscillator are

- Instead of using a large transformer, a single coil can be used as an auto-transformer.
- Frequency can be varied by employing either a variable capacitor or a variable inductor.
- Less number of components are sufficient.
- The amplitude of the output remains constant over a fixed frequency range.

Disadvantages

The disadvantages of Hartley oscillator are

- It cannot be a low frequency oscillator.
- Harmonic distortions are present.

Applications

The applications of Hartley oscillator are

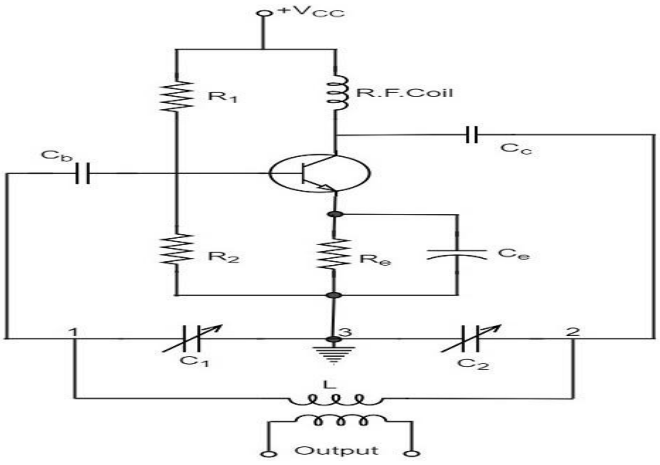
- It is used to produce a sine wave of desired frequency.
- Mostly used as a local oscillator in radio receivers.
- It is also used as R.F. Oscillator.

Colpitts Oscillator:

A Colpitts oscillator looks just like the Hartley oscillator but the inductors and capacitors are replaced with each other in the tank circuit. The constructional details and operation of a colpitts oscillator are as discussed below.

Construction

Let us first take a look at the circuit diagram of a Colpitts oscillator.



The resistors R_1, R_2 and R_e provide necessary bias condition for the circuit. The capacitor C_e provides a.c. ground thereby providing any signal degeneration. This also provides temperature stabilization. The capacitors C_c and C_b are employed to block d.c. and to provide an a.c. path. The radio frequency choke (R.F.C) offers very high impedance to high frequency currents which means it shorts for d.c. and opens for a.c. Hence it provides d.c. load for collector and keeps a.c. currents out of d.c. supply source.

Tank Circuit

The frequency determining network is a parallel resonant circuit which consists of variable capacitors C_1 and C_2 along with an inductor L. The junction of $C_1$and C_2 are earthed. The capacitor C_1 has its one end connected to base via C_c and the other to emitter via C_e. the voltage developed across C_1 provides the regenerative feedback required for the sustained oscillations.

Operation

When the collector supply is given, a transient current is produced in the oscillatory or tank circuit. The oscillatory current in the tank circuit produces a.c. voltage across C_1 which are applied to the base emitter junction and appear in the amplified form in the collector circuit and supply losses to the tank circuit. If terminal 1 is at positive potential with respect to terminal 3 at any instant, then terminal 2 will be at negative potential with respect to 3 at that instant because terminal 3 is grounded. Therefore, points 1 and 2 are out of phase by 180^o. As the CE configured transistor provides 180^o phase shift, it makes 360^ophase shift between the input and output voltages. Hence, feedback is properly phased to produce continuous Undamped oscillations. When the **loop gain |βA| of the amplifier is greater than one, oscillations are sustained** in the circuit.

Frequency

The equation for **frequency of Colpitts oscillator** is given as

$$f=12\pi LCT----\sqrt{}f=12\pi LCT$$

C_T is the total capacitance of C_1 and C_2 connected in series.

$$1CT=1C1+1C21CT=1C1+1C2$$
$$CT=C1\times C2C1+C2CT=C1\times C2C1+C2$$

Advantages

The advantages of Colpitts oscillator are as follows −

- Colpitts oscillator can generate sinusoidal signals of very high frequencies.
- It can withstand high and low temperatures.
- The frequency stability is high.
- Frequency can be varied by using both the variable capacitors.
- Less number of components are sufficient.
- The amplitude of the output remains constant over a fixed frequency range.

The Colpitts oscillator is designed to eliminate the disadvantages of Hartley oscillator and is known to have no specific disadvantages. Hence there are many applications of a colpitts oscillator.

Applications

The applications of Colpitts oscillator are as follows −

- Colpitts oscillator can be used as High frequency sine wave generator.
- This can be used as a temperature sensor with some associated circuitry.
- Mostly used as a local oscillator in radio receivers.
- It is also used as R.F. Oscillator.
- It is also used in Mobile applications.
- It has got many other commercial applications.

RC Phase shift oscillator:

One of the important features of an oscillator is that the feedback energy applied should be in correct phase to the tank circuit. The oscillator circuits discussed so far has employed inductor (L) and capacitor (C) combination, in the tank circuit or frequency determining circuit. We have observed that the LC combination in oscillators provide 180^o phase shift and transistor in CE configuration provide 180° phase shift to make a total of 360^o phase shift so that it would make a zero difference in phase.

Drawbacks of LC circuits

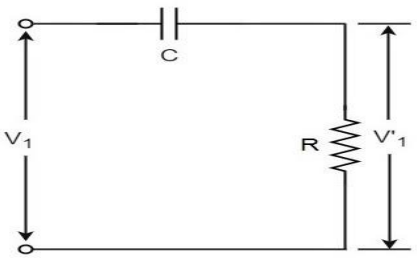
Though they have few applications, the **LC** circuits have few **drawbacks** such as

- Frequency instability
- Waveform is poor
- Cannot be used for low frequencies
- Inductors are bulky and expensive

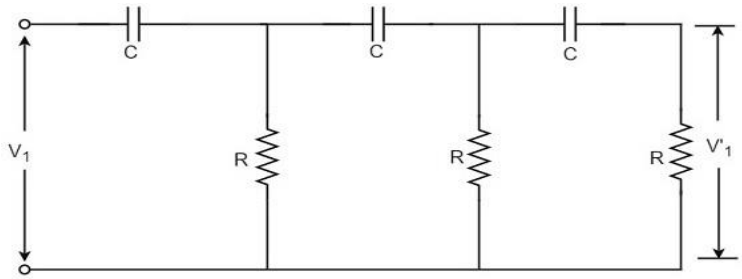
We have another type of oscillator circuits, which are made by replacing the inductors with resistors. By doing so, the frequency stability is improved and a good quality waveform is obtained. These oscillators can also produce lower frequencies. As well, the circuit becomes neither bulky nor expensive. All the drawbacks of **LC** oscillator circuits are thus eliminated in **RC** oscillator circuits. Hence the need for RC oscillator circuits arise. These are also called as **Phase–shift Oscillators**.

Principle of Phase-shift oscillators

We know that the output voltage of an RC circuit for a sine wave input leads the input voltage. The phase angle by which it leads is determined by the value of RC components used in the circuit. The following circuit diagram shows a single section of an RC network.



The output voltage V_1' across the resistor R leads the input voltage applied input V_1 by some phase angle ϕ^o. If R were reduced to zero, V_1' will lead the V_1 by 90^o i.e., $\phi^o = 90^o$. However, adjusting R to zero would be impracticable, because it would lead to no voltage across R. Therefore, in practice, R is varied to such a value that makes V_1' to lead V_1 by 60^o. The following circuit diagram shows the three sections of the RC network.



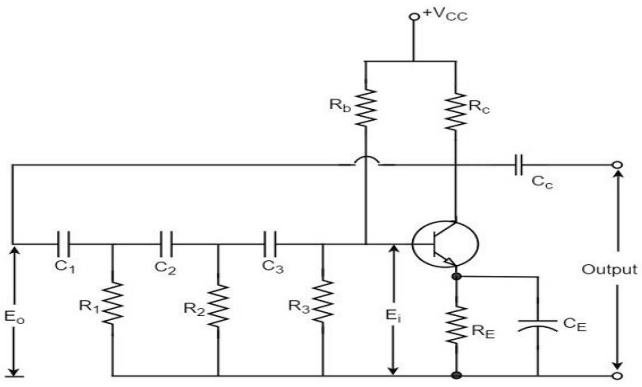
Each section produces a phase shift of 60^o. Consequently, a total phase shift of 180^o is produced, i.e., voltage V_2 leads the voltage V_1 by 180^o.

Phase-shift Oscillator Circuit

The oscillator circuit that produces a sine wave using a phase-shift network is called as a Phase-shift oscillator circuit.

Construction

The phase-shift oscillator circuit consists of a single transistor amplifier section and a RC phase-shift network. The phase shift network in this circuit, consists of three RC sections. At the resonant frequency f_o, the phase shift in each RC section is 60^o so that the total phase shift produced by RC network is 180^o. The following circuit diagram shows the arrangement of an RC phase-shift oscillator.



The frequency of oscillations is given by

$$fo=12\pi RC6–\sqrt{}fo=12\pi RC6$$

Where

$$R1=R2=R3=RR1=R2=R3=R$$
$$C1=C2=C3=CC1=C2=C3=C$$

Operation

The circuit when switched ON oscillates at the resonant frequency f_o. The output E_o of the amplifier is fed back to RC feedback network. This network produces a phase shift of 180^o and a voltage E_i appears at its output. This voltage is applied to the transistor amplifier.

The feedback applied will be

$$m=Ei/Eom=Ei/Eo$$

The feedback is in correct phase, whereas the transistor amplifier, which is in CE configuration, produces a 180^o phase shift. The phase shift produced by network and the transistor add to form a phase shift around the entire loop which is 360^o.

Advantages

The advantages of RC phase shift oscillator are as follows −

- It does not require transformers or inductors.
- It can be used to produce very low frequencies.
- The circuit provides good frequency stability.

Disadvantages

The disadvantages of RC phase shift oscillator are as follows −

- Starting the oscillations is difficult as the feedback is small.
- The output produced is small.

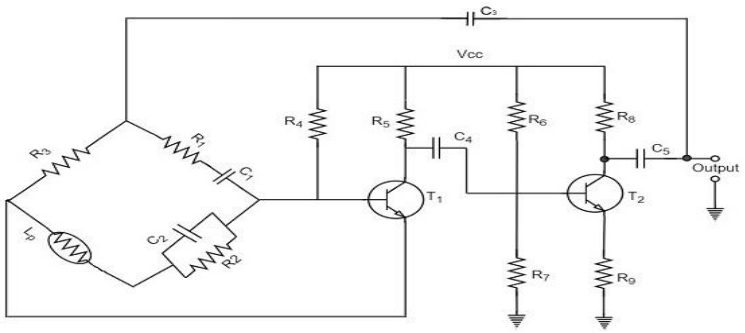
Wien bridge oscillator

Another type of popular audio frequency oscillator is the Wien bridge oscillator circuit. This is mostly used because of its important features. This circuit is free from the **circuit fluctuations** and the **ambient temperature**.

The main advantage of this oscillator is that the frequency can be varied in the range of 10Hz to about 1MHz whereas in RC oscillators, the frequency is not varied.

Construction

The circuit construction of Wien bridge oscillator can be explained as below. It is a two-stage amplifier with RC bridge circuit. The bridge circuit has the arms R_1C_1, R_3, R_2C_2 and the tungsten lamp L_p. Resistance R_3 and the lamp L_p are used to stabilize the amplitude of the output. The following circuit diagram shows the arrangement of a Wien bridge oscillator.



The transistor T_1 serves as an oscillator and an amplifier while the other transistor T_2 serves as an inverter. The inverter operation provides a phase shift of 180º. This circuit provides positive feedback through R_1C_1, C_2R_2 to the transistor T_1 and negative feedback through the voltage divider to the input of transistor T_2. The frequency of oscillations is determined by the series element R_1C_1 and parallel element R_2C_2 of the bridge.

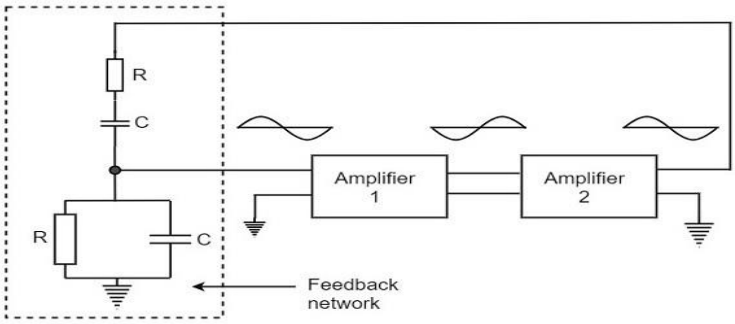
$$f=12\pi R1C1R2C2----------\sqrt{f=12\pi R1C1R2C2}$$

If $R_1 = R_2$ and $C_1 = C_2 = C$

Then,

$$f=12\pi RCf=12\pi RC$$

Now, we can simplify the above circuit as follows −



The oscillator consists of two stages of RC coupled amplifier and a feedback network. The voltage across the parallel combination of R and C is fed to the input of amplifier 1. The net phase shift through the two amplifiers is zero. The usual idea of connecting the output of amplifier 2 to amplifier 1 to provide signal regeneration for oscillator is not applicable here as the amplifier 1 will amplify signals over a wide range of frequencies and hence direct coupling would result in poor frequency stability. By adding Wien bridge feedback network, the oscillator becomes sensitive to a particular frequency and hence frequency stability is achieved.

Operation

When the circuit is switched ON, the bridge circuit produces oscillations of the frequency stated above. The two transistors produce a total phase shift of 360º so that proper positive feedback is ensured. The negative feedback in the circuit ensures constant output. This is achieved by temperature sensitive tungsten lamp L_p. Its resistance increases with current. If the amplitude of the output increases, more current is produced and more negative feedback is achieved. Due to this, the output would return to the original value. Whereas, if the output tends to decrease, reverse action would take place.

Advantages

The advantages of Wien bridge oscillator are as follows −

- The circuit provides good frequency stability.
- It provides constant output.
- The operation of circuit is quite easy.
- The overall gain is high because of two transistors.
- The frequency of oscillations can be changed easily.
- The amplitude stability of the output voltage can be maintained more accurately, by replacing R_2 with a thermistor.

Disadvantages

The disadvantages of Wien bridge oscillator are as follows −

- The circuit cannot generate very high frequencies.
- Two transistors and number of components are required for the circuit construction.

MODULE-V

OPERATIOANL AMPLIFIERS

Ideal op-amp, Output offset voltage, input bias current, input offset current, slew rate, gain bandwidth product, Inverting and non-inverting amplifier, Differentiator, integrator, Square-wave and triangular-wave generators.

Introduction to Operational amplifiers:

An **electronic circuit** is a group of electronic components connected for a specific purpose.

A simple electronic circuit can be designed easily because it requires few discrete electronic components and connections. However, designing a complex electronic circuit is difficult, as it requires more number of discrete electronic components and their connections. It is also time taking to build such complex circuits and their reliability is also less. These difficulties can be overcome with Integrated Circuits.

Integrated Circuit (IC)

If multiple electronic components are interconnected on a single chip of semiconductor material, then that chip is called as an **Integrated Circuit (IC)**. It consists of both active and passive components.

This chapter discusses the advantages and types of ICs.

Advantages of Integrated Circuits

Integrated circuits offer many advantages. They are discussed below −

- **Compact size** − For a given functionality, you can obtain a circuit of smaller size using ICs, compared to that built using a discrete circuit.
- **Lesser weight** − A circuit built with ICs weighs lesser when compared to the weight of a discrete circuit that is used for implementing the same function of IC. using ICs, compared to that built using a discrete circuit.
- **Low power consumption** − ICs consume lower power than a traditional circuit,because of their smaller size and construction.
- **Reduced cost** − ICs are available at much reduced cost than discrete circuits because of their fabrication technologies and usage of lesser material than discrete circuits.
- **Increased reliability** − Since they employ lesser connections, ICs offer increased reliability compared to digital circuits.
- **Improved operating speeds** − ICs operate at improved speeds because of their switching speeds and lesser power consumption.

Types of Integrated Circuits

Integrated circuits are of two types − **Analog Integrated Circuits and Digital Integrated Circuits**.

Analog Integrated Circuits

Integrated circuits that operate over an entire range of continuous values of the signal amplitude are called as **Analog Integrated Circuits.** These are further classified into the two types as discussed here −

- **Linear Integrated Circuits** − An analog IC is said to be Linear, if there exists a linear relation between its voltage and current. IC 741, an 8-pin Dual In-line Package (DIP)op-amp, is an example of Linear IC.
- **Radio Frequency Integrated Circuits** − An analog IC is said to be Non-Linear, if there exists a non-linear relation between its voltage and current. A Non-Linear IC is also called as Radio Frequency IC.

Digital Integrated Circuits

If the integrated circuits operate only at a few pre-defined levels instead of operating for an entire range of continuous values of the signal amplitude, then those are called as **Digital Integrated Circuits**.

Operational Amplifier, also called as an Op-Amp, is an integrated circuit, which can be used to perform various linear, non-linear, and mathematical operations. An op-amp is a **direct coupled high gain amplifier**. You can operate op-amp both with AC and DC signals. This chapter discusses the characteristics and types of op-amps.

Construction of Operational Amplifier

An op-amp consists of differential amplifier(s), a level translator and an output stage. A differential amplifier is present at the input stage of an op-amp and hence an op-amp consists of **two input terminals**. One of those terminals is called as the **inverting terminal** and the other one is called as the **non-inverting terminal**. The terminals are named based on the phase relationship between their respective inputs and outputs.

Characteristics of Operational Amplifier

The important characteristics or parameters of an operational amplifier are as follows −

- Open loop voltage gain
- Output offset voltage
- Common Mode Rejection Ratio
- Slew Rate

This section discusses these characteristics in detail as given below −

Open loop voltage gain

The open loop voltage gain of an op-amp is its differential gain without any feedback path.

Mathematically, the open loop voltage gain of an op-amp is represented as −

$$Av=v0v1−v2Av=v0v1−v2$$

Output offset voltage

The voltage present at the output of an op-amp when its differential input voltage is zero is called as **output offset voltage.**

Common Mode Rejection Ratio

Common Mode Rejection Ratio (**CMRR**) of an op-amp is defined as the ratio of the closed loop differential gain, AdAd and the common mode gain, AcAc.
Mathematically, CMRR can be represented as −

$$CMRR=AdAcCMRR=AdAc$$

Note that the common mode gain, AcAc of an op-amp is the ratio of the common mode output voltage and the common mode input voltage.

Slew Rate

Slew rate of an op-amp is defined as the maximum rate of change of the output voltage due to a step input voltage.

Mathematically, slew rate (SR) can be represented as −

$$SR=MaximumofdV0dtSR=MaximumofdV0dt$$

Where, V0V0 is the output voltage. In general, slew rate is measured in either V/μSecV/μSec or V/mSecV/mSec.

Types of Operational Amplifiers

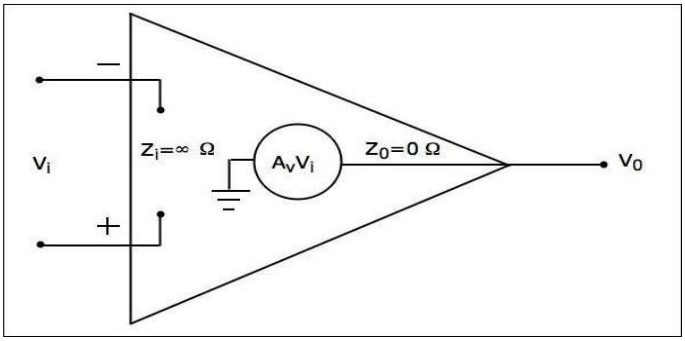
An op-amp is represented with a triangle symbol having two inputs and one output.

Op-amps are of two types: **Ideal Op-Amp** and **Practical Op-Amp**.

They are discussed in detail as given below −

Ideal Op-Amp

An ideal op-amp exists only in theory, and does not exist practically. The **equivalent circuit** of an ideal op-amp is shown in the figure given below −

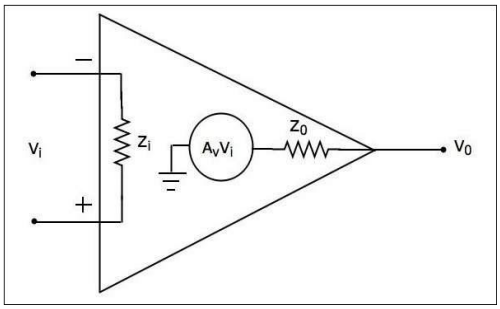


An **ideal op-amp** exhibits the following characteristics −

- Input impedance Zi=∞ΩZi=∞Ω
- Output impedance Z0=0ΩZ0=0Ω
- Open loop voltage gaine Av=∞Av=∞
- If (the differential) input voltage Vi=0VVi=0V, then the output voltage will be V0=0VV0=0V
- Bandwidth is **infinity**. It means, an ideal op-amp will amplify the signals of any frequency without any attenuation.
- Common Mode Rejection Ratio **(CMRR)** is **infinity**.
- Slew Rate **(SR)** is **infinity**. It means, the ideal op-amp will produce a change in the output instantly in response to an input step voltage.

Practical Op-Amp

Practically, op-amps are not ideal and deviate from their ideal characteristics because of some imperfections during manufacturing. The **equivalent circuit** of a practical op-amp is shown in the following figure −



A **practical op-amp** exhibits the following characteristics −

- Input impedance, ZiZi in the order of **Mega ohms**.
- Output impedance, Z0Z0 in the order of **few ohms.**.
- Open loop voltage gain, AvAv will be **high**.

When you choose a practical op-amp, you should check whether it satisfies the following conditions −

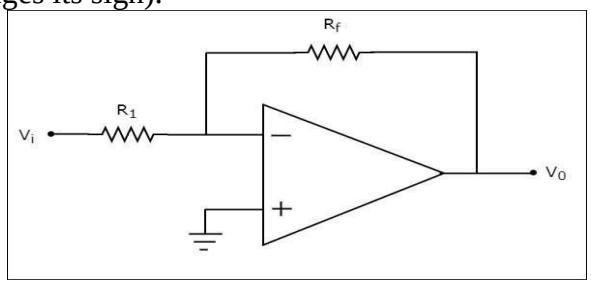
- Input impedance, ZiZi should be as high as possible.
- Output impedance, Z0Z0 should be as low as possible.
- Open loop voltage gain, AvAv should be as high as possible.
- Output offset voltage should be as low as possible.
- The operating Bandwidth should be as high as possible.
- CMRR should be as high as possible.
- Slew rate should be as high as possible.

A circuit is said to be **linear**, if there exists a linear relationship between its input and the output. Similarly, a circuit is said to be **non-linear**, if there exists a non-linear relationship between its input and output. Op-amps can be used in both linear and non-linear applications. The following are the basic applications of op-amp −

- Inverting Amplifier
- Non-inverting Amplifier
- Voltage follower

Inverting Amplifier

An inverting amplifier takes the input through its inverting terminal through a resistor R1R1, and produces its amplified version as the output. This amplifier not only amplifies the input but also inverts it (changes its sign).



Note that for an op-amp, the voltage at the inverting input terminal is equal to the voltage at its non-inverting input terminal. Physically, there is no short between those two terminals but **virtually**, they are in **short** with each other. In the circuit shown above, the non-inverting input terminal is connected to ground. That means zero volts is applied at the non-inverting input terminal of the op-amp. According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp will be zero volts.

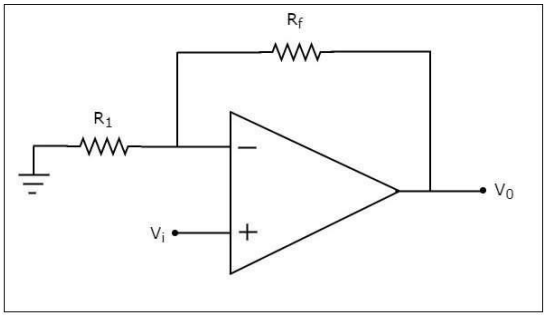
The **nodal equation** at this terminal's node is as shown below −

$$0-ViR1+0-V0Rf=00-ViR1+0-V0Rf=0$$
$$=>-ViR1=V0Rf=>-ViR1=V0Rf$$
$$=>V0=(-RfR1)Vt=>V0=(-RfR1)Vt$$
$$=>V0Vi=-RfR1=>V0Vi=-RfR1$$

The ratio of the output voltage V0V0 and the input voltage ViVi is the voltage-gain or gain of the amplifier. Therefore, the **gain of inverting amplifier** is equal to −RfR1−RfR1.
Note that the gain of the inverting amplifier is having a **negative sign**. It indicates that there exists a 180^0 phase difference between the input and the output.

Non-Inverting Amplifier

A non-inverting amplifier takes the input through its non-inverting terminal, and produces its amplified version as the output. As the name suggests, this amplifier just amplifies the input, without inverting or changing the sign of the output. The **circuit diagram** of a non-inverting amplifier is shown in the following figure −



In the above circuit, the input voltage ViVi is directly applied to the non-inverting input terminal of op-amp. So, the voltage at the non-inverting input terminal of the op-amp will be ViVi. By using **voltage division principle**, we can calculate the voltage at the inverting input terminal of the op-amp as shown below −

$$=>V1=V0(R1R1+Rf)=>V1=V0(R1R1+Rf)$$

According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp is same as that of the voltage at its non-inverting input terminal.

$$=>V1=Vi=>V1=Vi$$
$$=>V0(R1R1+Rf)=Vi=>V0(R1R1+Rf)=Vi$$
$$=>V0Vi=R1+RfR1=>V0Vi=R1+RfR1$$
$$=>V0Vi=1+RfR1=>V0Vi=1+RfR1$$

Now, the ratio of output voltage V0V0 and input voltage ViVi or the voltage-gain or **gain of the non-inverting amplifier** is equal to 1+RfR11+RfR1. Note that the gain of the non-inverting amplifier is having a **positive sign**. It indicates that there is no phase difference between the input and the output.

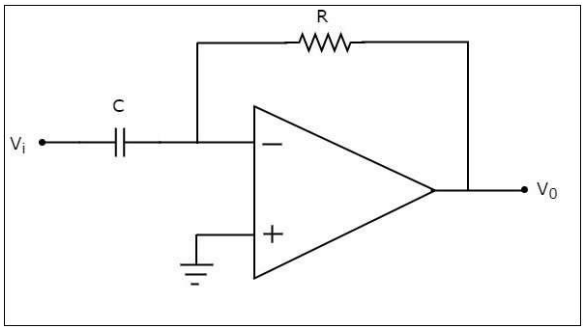
Integrator and Differentiator:

The electronic circuits which perform the mathematical operations such as differentiation and integration are called as differentiator and integrator, respectively. This chapter discusses in detail about op-amp based **differentiator** and integrator. Please note that these also come under linear applications of op-amp.

Differentiator

A **differentiator** is an electronic circuit that produces an output equal to the first derivative of its input. This section discusses about the op-amp based differentiator in detail.

An op-amp based differentiator produces an output, which is equal to the differential of input voltage that is applied to its inverting terminal. The **circuit diagram** of an op-amp based differentiator is shown in the following figure −



In the above circuit, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied to its non-inverting input terminal.

According to the **virtual short concept**, the voltage at the inverting input terminal of opamp will be equal to the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal of op-amp will be zero volts.

The nodal equation at the inverting input terminal's node is −

$$Cd(0-Vi)dt+0-V0R=0Cd(0-Vi)dt+0-V0R=0$$
$$=>-CdVidt=V0R=>-CdVidt=V0R$$
$$=>V0=-RCdVidt=>V0=-RCdVidt$$

If RC=1secRC=1sec, then the output voltage V0V0 will be −

$$V0=-dVidtV0=-dVidt$$

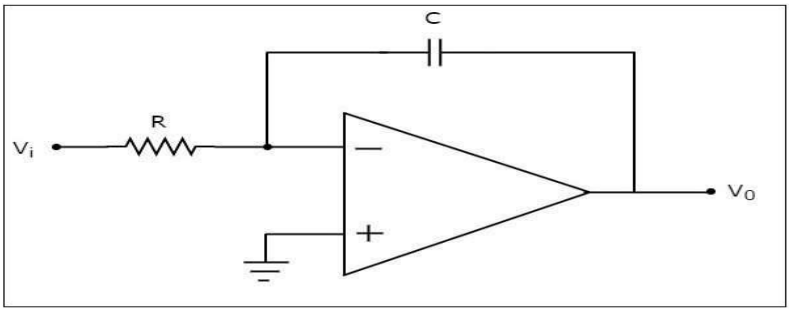
Thus, the op-amp based differentiator circuit shown above will produce an output, which is the differential of input voltage ViVi, when the magnitudes of impedances of resistor and capacitor are reciprocal to each other.

Note that the output voltage V0V0 is having a **negative sign**, which indicates that there exists a 180^0 phase difference between the input and the output.

Integrator

An **integrator** is an electronic circuit that produces an output that is the integration of the applied input. This section discusses about the op-amp based integrator.

An op-amp based integrator produces an output, which is an integral of the input voltage applied to its inverting terminal. The **circuit diagram** of an op-amp based integrator is shown in the following figure −



In the circuit shown above, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied to its non-inverting input terminal. According to **virtual short concept**, the voltage at the inverting input terminal of op-amp will be equal to the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal of op-amp will be zero volts.

The **nodal equation** at the inverting input terminal is −

$$0-ViR+Cd(0-V0)dt=00-ViR+Cd(0-V0)dt=0$$
$$=>-ViR=CdV0dt=>-ViR=CdV0dt$$
$$=>dV0dt=-ViRC=>dV0dt=-ViRC$$
$$=>dV0=(-ViRC)dt=>dV0=(-ViRC)dt$$

Integrating both sides of the equation shown above, we get −

$$\int dV0=\int(-ViRC)dt\int dV0=\int(-ViRC)dt$$
$$=>V0=-1RC\int Vtdt=>V0=-1RC\int Vtdt$$

If RC=1secRC=1sec, then the output voltage, V0V0 will be −

$$V0=-\int VidtV0=-\int Vidt$$

So, the op-amp based integrator circuit discussed above will produce an output, which is the integral of input voltage ViVi, when the magnitude of impedances of resistor and capacitor are reciprocal to each other.

Note − The output voltage, V0V0 is having a **negative sign**, which indicates that there exists 180^0 phase difference between the input and the output.

Waveform Generators:

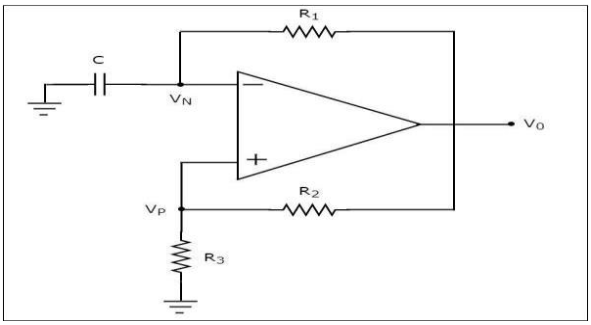
A **waveform generator** is an electronic circuit, which generates a standard wave. There are two types of op-amp based waveform generators −

- Square wave generator
- Triangular wave generator

Square Wave Generator:

A **square wave generator** is an electronic circuit which generates square wave. This section discusses about op-amp based square wave generators.

The **circuit diagram** of a op-amp based square wave generator is shown in the following figure

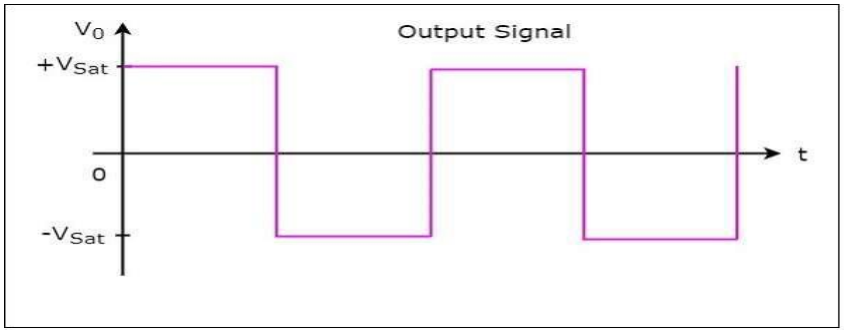


Observe that in the circuit diagram shown above, the resistor R1R1 is connected between the inverting input terminal of the op-amp and its output of op-amp. So, the resistor R1R1 is used in the **negative feedback**. Similarly, the resistor R2R2 is connected between the noninverting input terminal of the op-amp and its output. So, the resistor R2R2 is used in the **positive feedback** path. A capacitor C is connected between the inverting input terminal of the op-amp and ground. So, the **voltage across capacitor C** will be the input voltage at this inverting terminal of op-amp. Similarly, a resistor R3R3 is connected between the non-inverting input terminal of the op-amp and ground. So, the **voltage across resistor** R3R3 will be the input voltage at this non-inverting terminal of the op-amp.

The **operation** of a square wave generator is explained below −

- Assume, there is **no charge** stored in the capacitor initially. Then, the voltage present at the inverting terminal of the op-amp is zero volts. But, there is some offset voltage at non-inverting terminal of op-amp. Due to this, the value present at the output of above circuit will be +Vsat+Vsat.
- Now, the capacitor C starts **charging** through a resistor R1R1. The value present at the output of the above circuit will change to −Vsat−Vsat, when the voltage across the capacitor C reaches just greater than the voltage (positive value) across resistor R3R3.
- The capacitor C starts **discharging** through a resistor R1R1, when the output of above circuit is −Vsat−Vsat. The value present at the output of above circuit will change to +Vsat+Vsat,when the voltage across capacitor C reaches just less than (more negative) the voltage (negative value) across resistor R3R3.

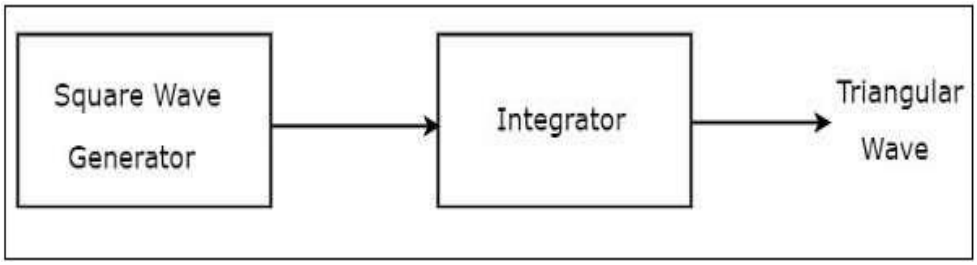
Thus, the circuit shown in the above diagram will produce a **square wave** at the output as shown in the following figure −



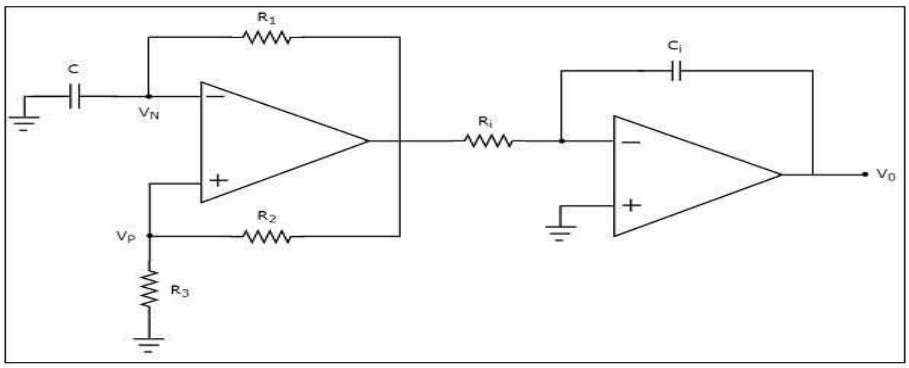
From the above figure we can observe that the output of square wave generator will have one of the two values: +Vsat+Vsat and −Vsat−Vsat. So, the output remains at one value for some duration and then transitions to another value and remains there for some duration. In this way, it continues.

Triangular Wave Generator:

A triangular wave generator is an electronic circuit, which generates a triangular wave. The **block diagram** of a triangular wave generator is shown in the following figure −



The block diagram of a triangular wave generator contains mainly two blocks: a square wave generator and an integrator. These two blocks are **cascaded**. That means, the output of square wave generator is applied as an input of integrator. Note that the integration of a square wave is nothing but a triangular wave. The **circuit diagram** of an op-amp based triangular wave generator is shown in the following figure −



We have already seen the circuit diagrams of a square wave generator and an integrator. Observe that we got the above **circuit diagram** of an op-amp based triangular wave generator by replacing the blocks with the respective circuit diagrams in the block diagram of a triangular wave generator.