DIGITAL SYSTEM DESIGN LABORATORY

III Semester: ECE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AECB10	Core	-	-	2	1	30	70	100
Contact Classes: Nil	Tutorial Classes: Nil	Practical Classes: 24				Total Classes: 24		

I. COURSE OVERVIEW:

The laboratory strives in exploring the logic design and related fields. Digital logic testers are used to provide students with practical training and familiarize themselves with the various functions of logic gates and using integrated components to complete circuitry functions and develop an interest in digital logic and enlighten them in the abilities of deduction. The lab allows students to conduct actual gate-level experiments on combinational and sequential circuits to increase student interest and develop skills to design digital gates using VHDL.

II. OBJECTIVES:

The course should enable the students to:

I Design and simulate the combinational logic circuits using HDL code.

II Model the sequential circuits and simulate using HDL code.

III Implementation of basic real time applications and verify the outputs using FPGA.

III. COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO 1	**Apply** the concept of Boolean algebra to verify the truth table ofvarious expressions using logic gates in Hardware Description Language.	Apply
CO 2	**Make use** of dataflow, structural and behavioral modeling styles of HDL for simulating the combinational logic circuits.	Apply
CO 3	**Analyze** the SR flip flop, JK flip flop, D flip flop, T flip flops for functional simulation and timing analysis.	analyze
CO 4	**Build** the universal shift registers, counters using the flip flops.	Apply
CO 5	**Examine** a finite state machine for detection of sequence.	Apply
CO 6	**Design** the real time applications like traffic light controller, chess clock controller FSM, elevator operations using FPGA kit.	Create

IV. SYLLABUS:

LIST OF EXPERIMENTS

WEEK - l	**REALIZATION OF A BOOLEAN FUNCTION**
Design and simulate the HDL code to realize three and three variable Boolean functions	
WEEK-2	**DESIGN OF DECODER AND ENCODER**
Design and simulate the HDL code for the following combinational circuits 3 to 8 Decoder 8 to 3 Encoder (With priority and without priority)	
WEEK-3	**DESIGN OF MULTIPLEXER AND DEMULTIPLEXER**
Design and simulate the HDL code for the following combinational circuits	

Multiplexer De-multiplexer	
WEEK -4	**DESIGN OF CODE CONVERTERS**
Design and simulate the HDL code for the following combinational circuits 4 - Bit binary to gray code converter 4 - Bit gray to binary code converter Comparator	
WEEK -5	**FULL ADDER AND FULL SUBTRACTOR DESIGN MODELING**
Write a HDL code to describe the functions of a full Adder and full subtractor using three modeling styles	
WEEK -6	**DESIGN OF 8-BIT ALU**
Design a model to implement 8-bit ALU functionality	
WEEK -7	**HDL MODEL FOR FLIP FLOPS**
Write HDL codes for the flip-flops - SR, D, JK, T	
WEEK -8	**DESIGN OF COUNTERS**
Write a HDL code for the following counters Binary counter BCD counter (Synchronous reset and asynchronous reset)	
WEEK-9	**HDL CODE FOR UNIVERSAL SHIFT REGISTER**
Design and simulate the HDL code for universal shift register	
WEEK-l0	**HDL CODE FOR CARRY LOOK AHEAD ADDER**
Design and simulate the HDL code for carry look ahead adder	
WEEK-l1	**HDL CODE TO DETECT A SEQUENCE**
Write a HDL code to detect the sequence 1010101 and simulate the code	
WEEK-l2	**CHESS CLOCK CONTROLLER FSM USING HDL**
Design a chess clock controller FSM using HDL and simulate the code	
WEEK-l3	**TRAFFIC LIGHT CONTROLLER USING HDL**
Design a traffic light controller using HDL and simulate the code	
WEEK-l4	**ELEVATOR DESIGN USING HDL CODE**
Write HDL code to simulate Elevator operations and simulate the code	

Reference Books:

1. Samir Palnitkar , “Verilog HDL: “A Guide to Digital Design and Synthesis”, Sun Microsystems Press, 2nd Edition, 2003.
2. T.R. Padmanabhan, B. Bala Tripura Sundari, “Design Through Verilog HDL”, New Jersey, Wiley-IEEE Press, 2009. ISBN: 978-0-471-44148-9
3. Zainalabedin Navabi, “Verilog Digital System Design”, TMH, 2nd Edition, 2008.

4. Peter Minns, Ian Elliott, "FSM-based Digital Design using Verilog HDL", John Wiley & Sons Ltd, 2008.

Web References:

1. https://inst.eecs.berkeley.edu/~cs150/fa06/Labs/verilog-ieee.pdf
2. http://www.asic-world.com/ www.sxecw.edu.in

SOFTWARE AND HARDWARE REQUIREMENTS FOR A BATCH OF 36 STUDENTS:

HARDWARE: Desktop Computer Systems 36 nos

SOFTWARE: Xilinx