



COMPUTER SCIENCE AND ENGINEERING (CYBER SECURITY)

ATTAINMENT OF COURSE OUTCOME - ACTION TAKEN REPORT

Name of the faculty:	Mr. S LAKSHMANA CHARI	Department:	Computer Science and Engineering (Cyber Security)
Regulation:	IARE - R20	Batch:	2021-2025
Course Name:	Computer Organization and Architecture	Course Code:	ACSC07
Semester:	III	Target Value:	60% (1.8)

Attainment of COs:

Course Outcome	Direct Attainment	Indirect Attainment	Overall Attainment	Observation
CO1 Illustrate interaction of components in a computer system with functional units and levels of programming languages	0.60	2.00	0.9	Not Attained
CO2 Demonstrate the implementation of micro-operations with the help of register transfer language and electronic circuits.	0.60	2.00	0.9	Not Attained
CO3 Identify appropriate addressing modes for specifying the location of an operand.	0.90	2.10	1.1	Not Attained
CO4 Make use of number system for data representation and binary arithmetic in digital computers.	0.90	2.00	1.1	Not Attained
CO5 Interpret the design of hardwired and micro-programmed control unit for execution of micro programs.	0.60	2.10	0.9	Not Attained
CO6 Summarize the concepts of pipelining and inter process communication for advanced processor design.	0.60	2.10	0.9	Not Attained

Action Taken Report: (To be filled by the concerned faculty / course coordinator)

CO1: Additional inputs will be provided on the concepts of basic organization of a computer for more practice.

CO2: Giving assignments and conducting tutorials on the concepts of micro-operations and register transfer languages for more practice.

CO3: Additional inputs will be provided on the concept of addressing modes for improving students performance.

CO4: Giving assignments and conducting tutorials on the concepts of number systems and data representation and binary arithmetic in digital computers.

CO5: Giving assignments and conducting tutorials on the concepts of design of hardwired and micro-programmed control unit for execution of micro programs for more practice.

CO6: Conducting guest lectures on concepts of pipelining and inter process communication for advanced processor design for improving students performance.

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