Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC002

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

B.Tech III Semester End Examinations (Supplementary) - January/February, 2018

Regulation: IARE – R16

DIGITAL SYSTEM DESIGN

(Electronics and Communication Engineering))

Time: 3 Hours **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) If a hamming code is constructed using even parity and the received code is 1110110.Detect and correct errors if any. **[7M]**

   (b) Convert the following into Excess-3 Code **[7M]**

   i. $(4B9)_{16}$

   ii. $(58)_{10}$

2. (a) Convert the following. **[7M]**

   i. $(4C9)_{16} = (\ )_8$

   ii. $(11011.11)_2 = (\ )_{10}$

   (b) Represent the following decimal numbers in BCD format **[7M]**

   (i) 9

   (iii) 25

UNIT – II

3. (a) Use the tabular method obtain the minimal expression for **[7M]**
   $F(A,B,C,D) = \sum m(0,1,5,7,8,10,14,15)$

   (b) What are the limitations of K-Maps. **[7M]**

4. (a) Minimize the following expressions using K-Map and implement using logic gates.
   F(A,B,C,D)= $\sum$(0,1,5,7,8,10,14,15) **[7M]**

   (b) Convert the following Sum of Product(SOP) to Product of Sums(POS) **[7M]**

$$F(A,B,C) = A'BC' + ABC + A'B'C + AB'C + ABC'$$

UNIT – III

5. (a) Design 3-bit binary to gray code converter using basic gates , NAND gates and NOR gates. **[7M]**

   (b) Design full adder combinational logic network using minimum number of NAND gates only. **[7M]**

6. (a) Design a combinational circuit whose output is true for two bit BCD input. **[7M]**

   (b) Design two bit BCD adder and explain its operation. **[7M]**

UNIT – IV

7. (a) Convert J-K Flip-Flop to S-R Flip-Flop. **[7M]**

   (b) With the help of logic Diagram and Functional Table explain the operation of 4-bit Johnson counter **[7M]**

8. (a) Sketch the logic networks for MOD-5 Johnson counter and explain its operation. **[7M]**

   (b) Design a Mod-6 Synchronous counter using clocked T flip-flops. **[7M]**

UNIT – V

9. (a) Differentiate between Mealy Machine and Moore Machine. **[7M]**

   (b) Minimize the State Table using Partition Technique as shown in Table-1 **[7M]**

Table 1

PS	NS,Z	
	X=0	X=1
A	E,0	D,1
B	F,0	D,0
C	E,0	B,1
D	F,0	B,0
E	C,0	F,1
F	B,0	C,0

10. (a) Write the state table for the state diagram shown in figure-1 **[7M]**

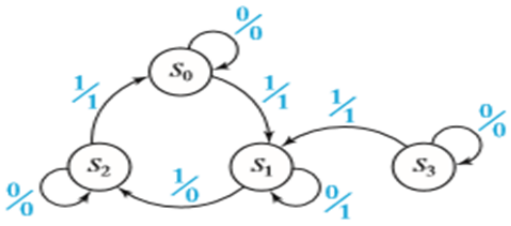

Figure 1

   (b) With an example, explain what is state reduction and also mention its advantages **[7M]**

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