Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC002

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

B.Tech III Semester End Examinations (Regular) - December, 2017

Regulation: IARE – R16

DIGITAL SYSTEM DESIGN

(Electronics and Communication Engineering))

Time: 3 Hours **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Perform the following. **[7M]**
   i. $(988.85)_{10} = (?)_{16} = (?)_2$
   ii. $(11101010.01011)_2 = (?)_{10} = (?)_{16}$
   (b) Distinguish between weighted and non-weighted codes with suitable example. **[7M]**

2. (a) Generate a 7 bit odd parity Hamming Code for the given 4 bit data word 1101. **[7M]**
   (b) Perform the following. **[7M]**
   i)10101001-10010011 using 2's complement method
   ii)(650)-(335)BCD subtraction using 9's complement method.

UNIT – II

3. (a) Discuss the properties of Boolean algebra. **[7M]**
   (b) Design the combinational logic circuit to convert BCD code to Excess-3 code and draw the circuit diagram using minimum number of NAND gates only. **[7M]**

4. (a) Define combinational logic circuit. Design 3-bit parity generator/checker (output is high for odd number of inputs and low for even number of inputs) using NOR gates only. **[7M]**
   (b) Use Quine-Mcluskey minimization technique, obtain the minimal sum expression for the Boolean function $f(a,b,c,d) = \sum m(6,7,9,10,13) + \sum d(1,4,5,11,15)$. **[7M]**

UNIT – III

5. (a) Write the truth table for a binary full subtractor function and obtain the irredundant disjunctive normal expressions for the function. Show how the function could be realized using minimum number of NAND gates. **[7M]**
   (b) Design 4-bit carry look ahead adder network and write its important merits. **[7M]**

6. (a) Design an EX-OR and EX-NOR Gate using NAND Gates **[7M]**
   (b) Describe the 4-bit serial adder using full adder with block diagram and illustrate with example. **[7M]**

UNIT – IV

7. (a) Explain the operation of Master slave JKFF using logic circuit, function table and timing diagram. **[7M]**

   (b) Draw the logic diagram for 4-bit universal shift register to perform the following operations, illustrate this register operation with suitable example. **[7M]**

MODE s1 s0	OPERATION
0 0	Hold
0 1	Shift Left
1 0	Shift Right
1 1	Parallel Load

8. (a) State and Derive the characteristic eqations for TFF, SRFF and JKFF. **[7M]**

   (b) Design a MOD-5 Synchronous counter using clocked D-FF for the sequence 0, 4, 1, 2, 3, 0, 4, ... **[7M]**

UNIT – V

9. (a) Design Mealy sequential network for the following sequence, output is high for non zero present state when input x =0 using edge triggered JKFF. $0 \rightarrow 1 \rightarrow 2 \;\; for\; x = 0, \;\; 0 \rightarrow 2 \rightarrow 1 \;\; for\; x = 1.$ **[7M]**

   (b) Construct the excitation table, transition table, state table and state diagram for the Moore sequential circuit expression **[7M]**

   $J_A = B,\; K_A = BX,\; J_B = X,\; K_B = A \oplus X$ *and output* $Y = A \oplus B.$

10. (a) Describe Mealy and Moore sequential circuit models with neat block diagrams. Compare. **[7M]**

    (b) Design a Moore type sequence detector to detect a serial input sequence of 101. **[7M]**

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