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INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Four Year B.Tech III Semester End Examinations (Supplementary) - July, 2018

Regulation: IARE – R16

DIGITAL SYSTEM DESIGN

Time: 3 Hours

(ECE)

Max Marks: 70

Answer ONE Question from each Unit

All Questions Carry Equal Marks

All parts of the question must be answered in one place only

UNIT – I

1. (a) Generate a 7 bit odd parity Hamming Code for the given 4 bit data word 1101. [7M]
- (b) Convert the following into Gray Code [7M]
 - i. $(3A8)_{16}$
 - ii. $(578)_8$
2. (a) Convert the following Binary numbers to Decimal and then to Hexadecimal. [7M]
 - i. 1010
 - ii. 1011.11
 - iii. 1101101
- (b) Distinguish between weighted and non-weighted codes with suitable example. [7M]

UNIT – II

3. (a) State and prove the De-Morgans theorem. [7M]
- (b) Solve(Simplify) the following Boolean equation Using Quine-McClusky technique $H = f(a, b, c, d) = \sum m(0,1,2,4,5,6,8,9,12,13)$. [7M]
4. (a) Define canonical form? Translate the following expressions into canonical form: [7M]
 - i) $f(a, b, c, d) = a'bc + a'c + bcd$
 - ii) $F(x, y, z) = (x' + y')(y + z')$
- (b) Get the minimized sum-of products expression for $N = f(a, b, c, d) = \prod (0, 1, 5, 6, 7, 8, 9)$ with don't cares: $\prod X(10, 11, 12, 13, 14, 15)$. Use Karnaugh map for simplification and write PIs and EPIs. [7M]

UNIT – III

5. (a) Implement a Full Subtractor using Half Subtractor and one OR Gate [7M]
- (b) Design a 4 bit BCD to Excess-3 Code Converter using Logic gates. [7M]
6. (a) Design a 4 Bit Prime Number Detector using Logic gates [7M]
- (b) Describe the 4-bit serial adder using full adder with block diagram and illustrate with example. [7M]

UNIT – IV

7. (a) Draw the circuit diagram of T Flip-Flop using NAND gates and explain its operation with the help of functional table. [7M]
(b) Design a Mod-12 Asynchronous Counter using J-K-Flip-Flop [7M]
8. (a) Convert D Flip-Flop to J-K Flip-Flop [7M]
(b) With the help of logic Diagram and Functional Table explain the operation of 4-bit Bidirectional Shift Registers [7M]

UNIT – V

9. (a) Explain Mealy and Moore models with general block diagrams. [7M]
(b) Design a Mealy type sequence detector to detect a serial input sequence of 101. [7M]
10. (a) Construct the excitation table, transition table, state table and state diagram for the Mealy sequential circuit shown. [7M]
(b) Design Moore sequential network for the following sequence, output is high for non zero present state irrespective of the x input using edge triggered JKFF. $0 \rightarrow 1 \rightarrow 2 \rightarrow 0$ for the input $x=1$, $0 \rightarrow 2 \rightarrow 1 \rightarrow 0$ for the input $x=0$. [7M]

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